

CALL FOR THESIS

QNANO Thesis Proposals

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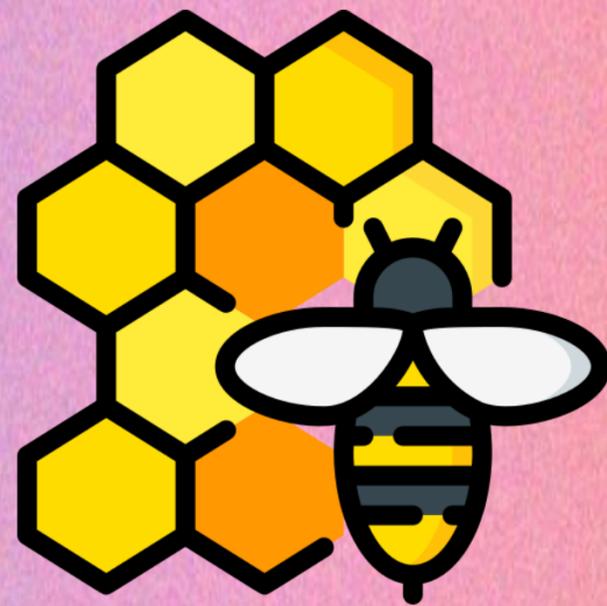
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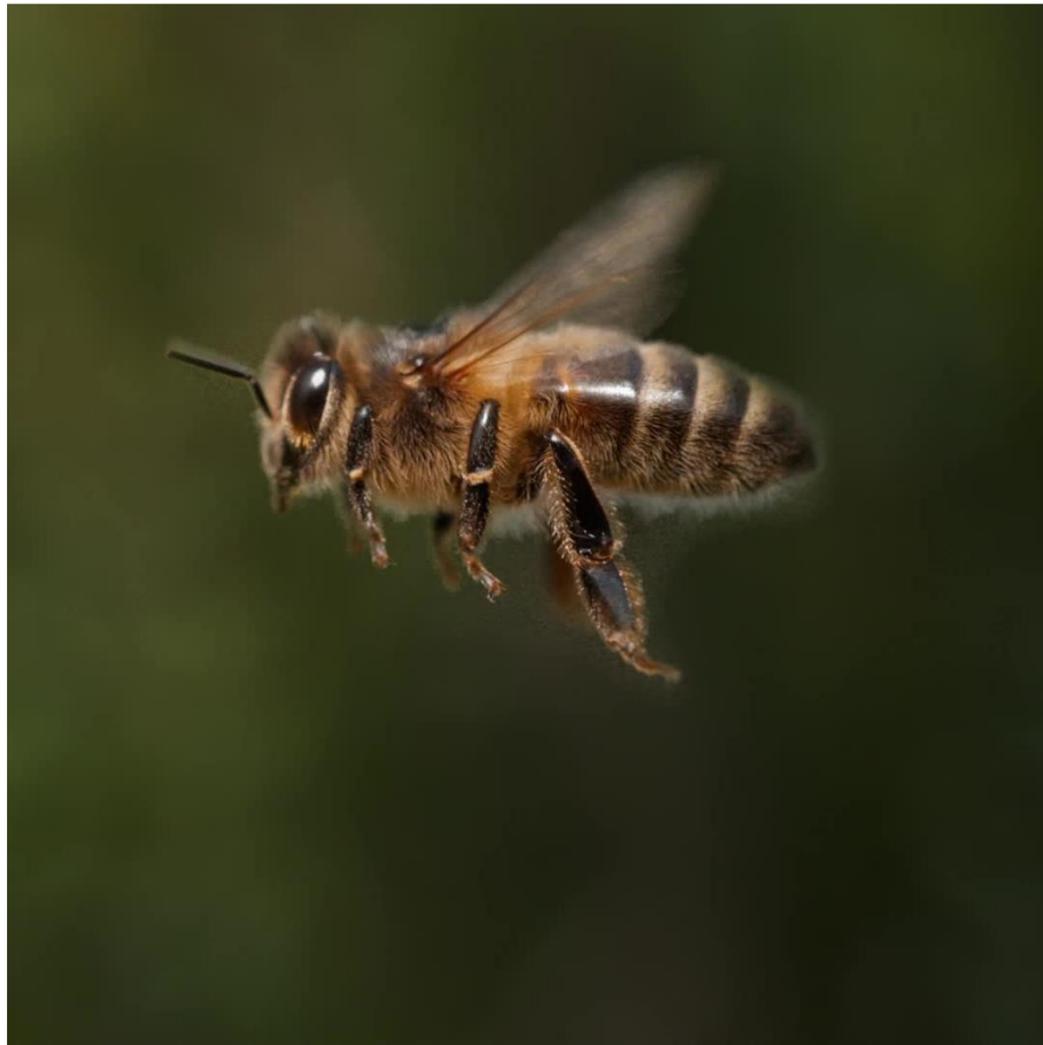
SMART AGRICULTURE: precision beekeeping



The Importance of Bees



Queen bee presence detection



- Presence of the queen bee is an important indicator of the health status of the bee colony
- Hives are often situated in remote locations
- Sound produced by buzzing of bees can serve as an indicator of bee activity



Our System



Custom non-invasive board integrable in beehives



Tiny Machine Learning model to predict queen bee presence on the edge



Low power IoT system powered by battery which lasts several years

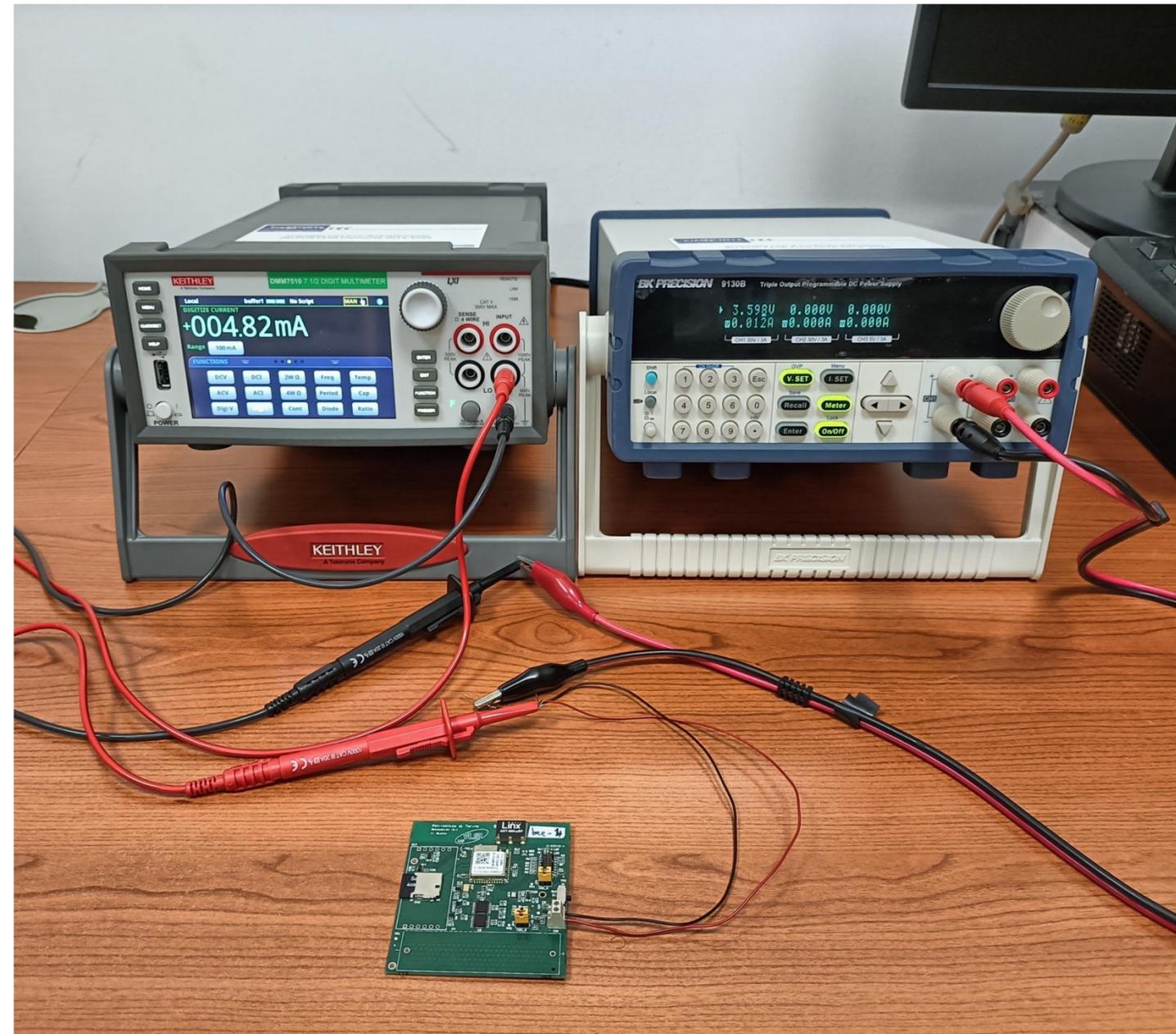


Queen bee presence and hive data are sent by a long-range wireless transmission and consultable remotely

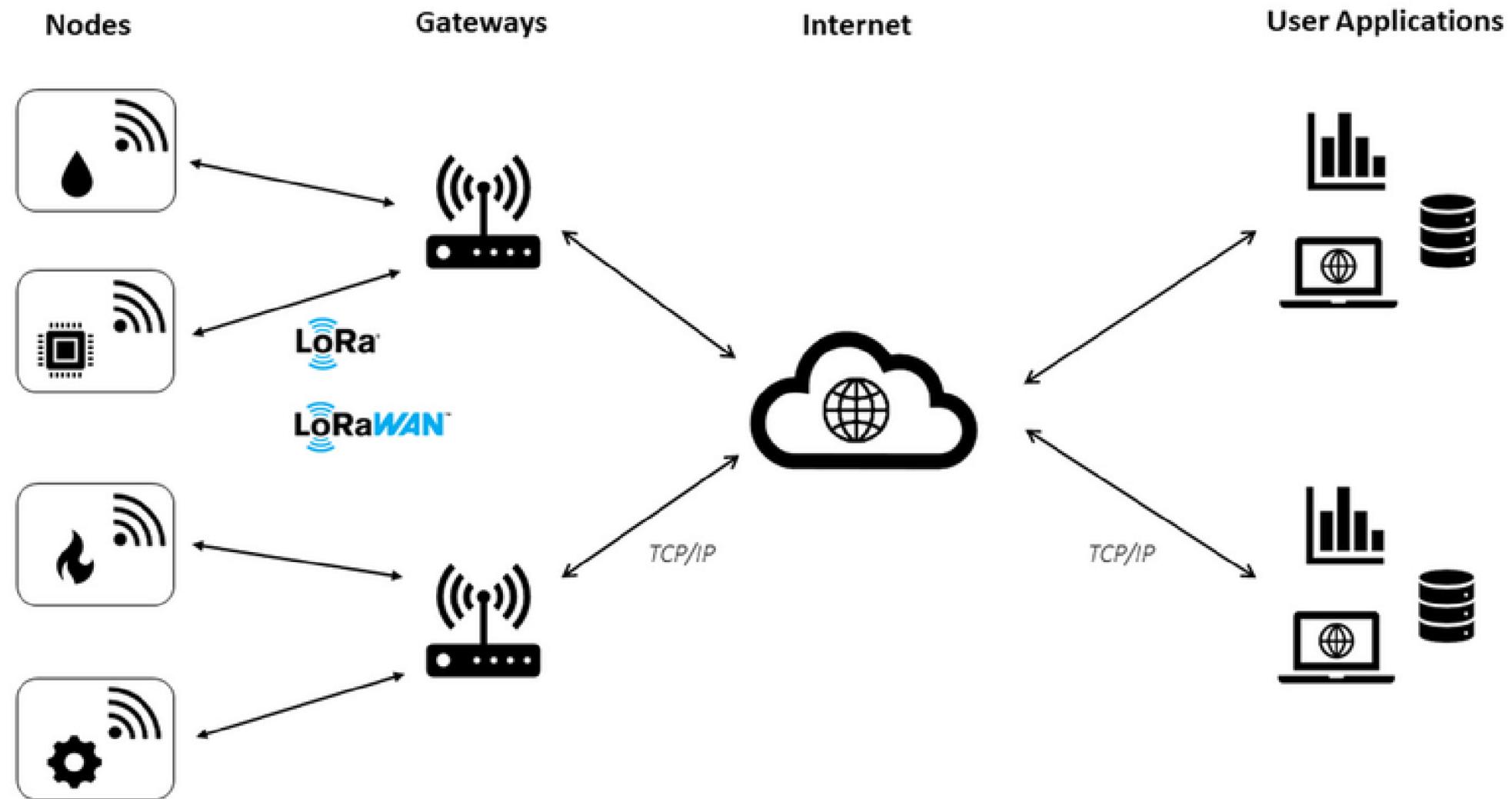


Board developed @VLSI Lab

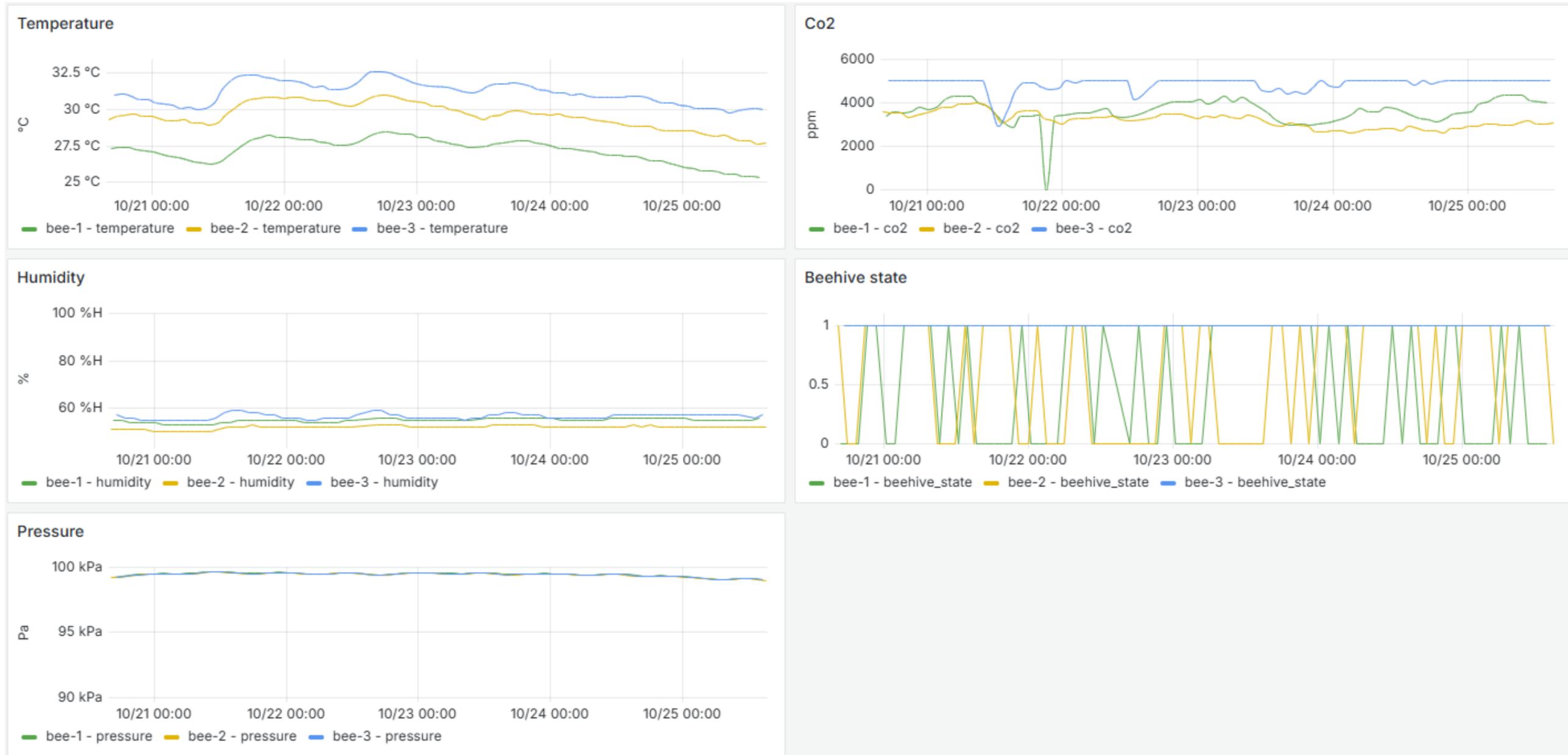
Measures



Remote monitoring system

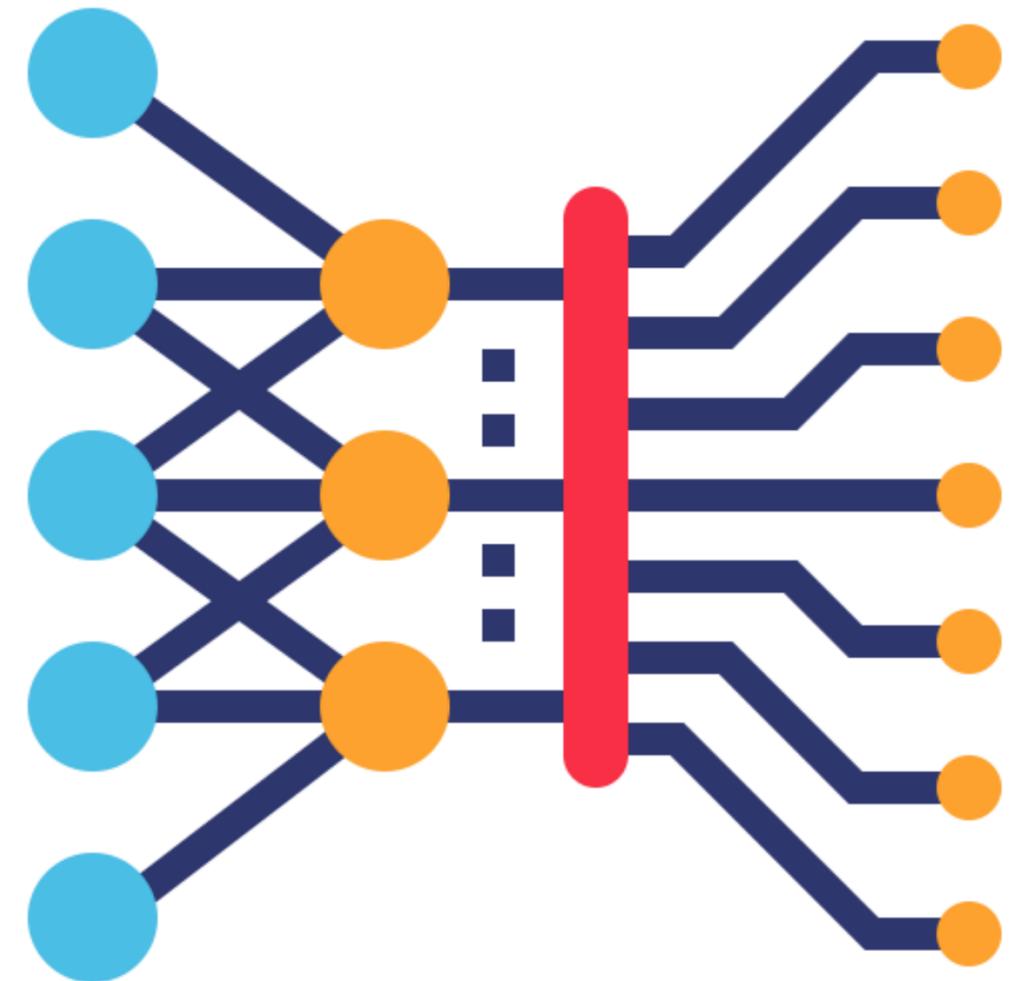


What we're able to monitor: the interface

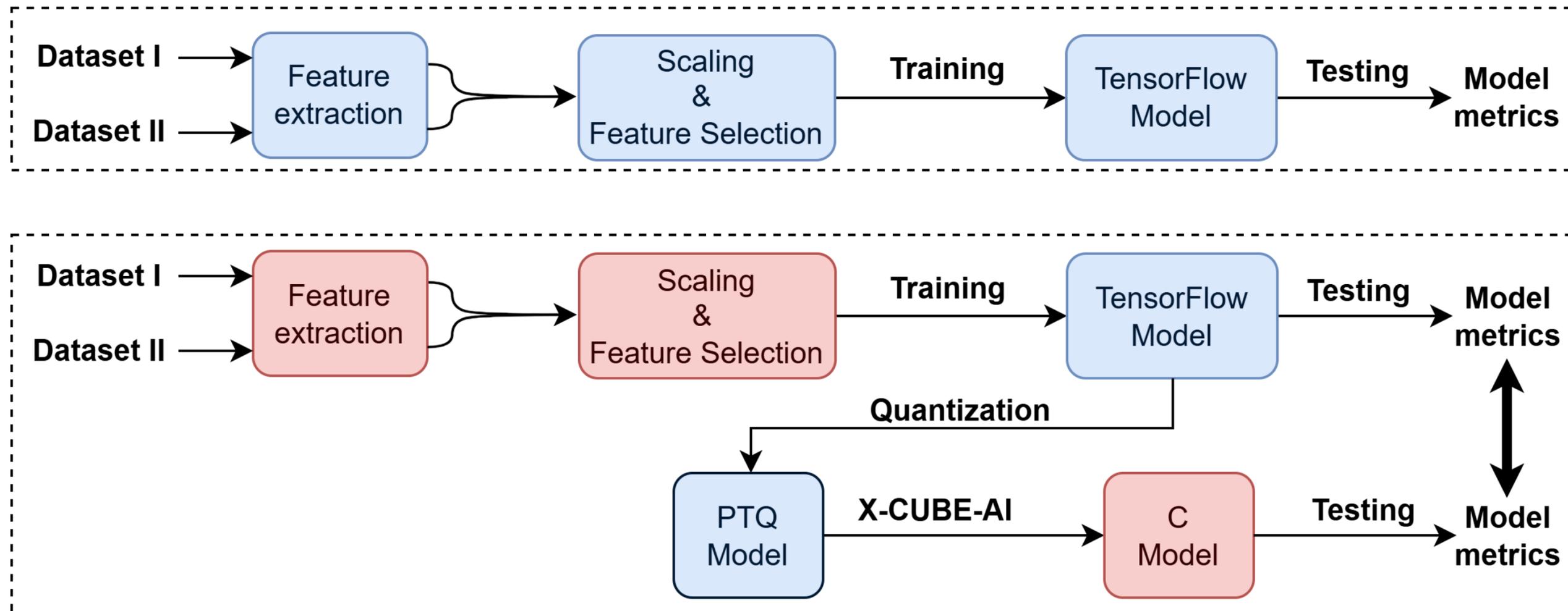


Machine Learning Enhancement

- Short Time Fourier Transform (**STFT**) and Mel-Frequency Cepstral Coefficients (**MFCC**) are used as features to infer queen bee presence
- High computational effort for feature extraction
- Convolutional Neural Networks achieve up to 99% of accuracy
- Models with millions of parameters
- **Difficult to deploy on an embedded device**



Framework and Methodology



MFCC Quantized model metrics

FFT	Audio length	Accuracy [%] MELS		
		10	20	30
512	3 seconds	90,09	93,13	94,85
	5 seconds	90,55	93,52	95,63
1024	3 seconds	90,40	95,55	95,32
	5 seconds	91,26	95,55	96,64

- + MFCC provide better compression and **int16** precision achieve good performance
- + Small accuracy drop for 20 and 30 MELS compared to floating point model
- + Slight accuracy improvement using 5 second audio



Precision Apiculture

Description:

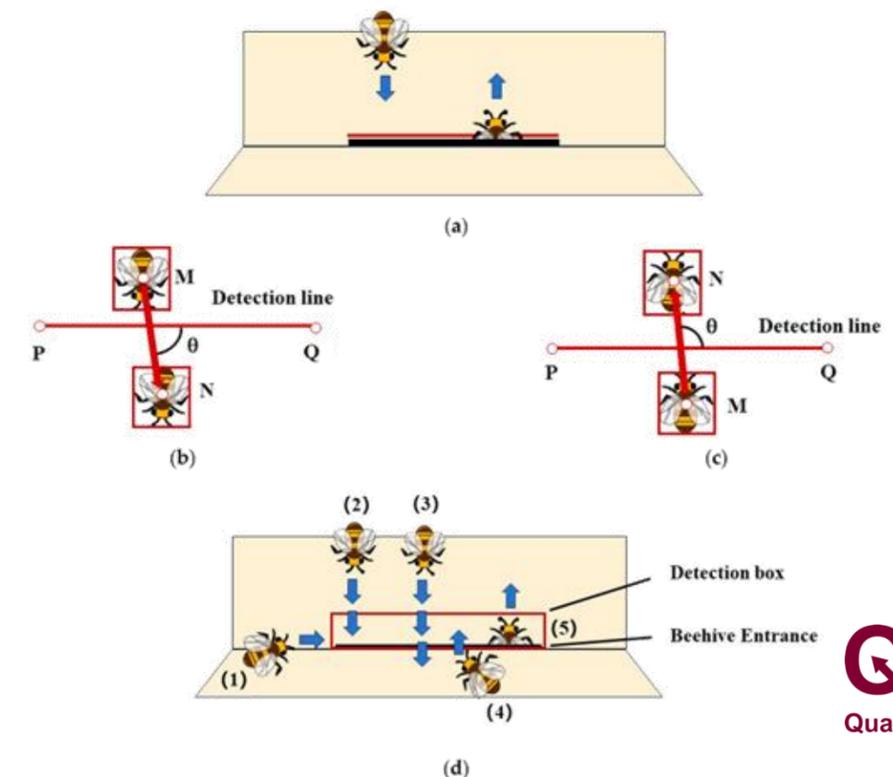
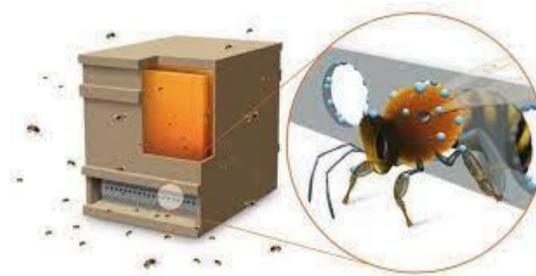
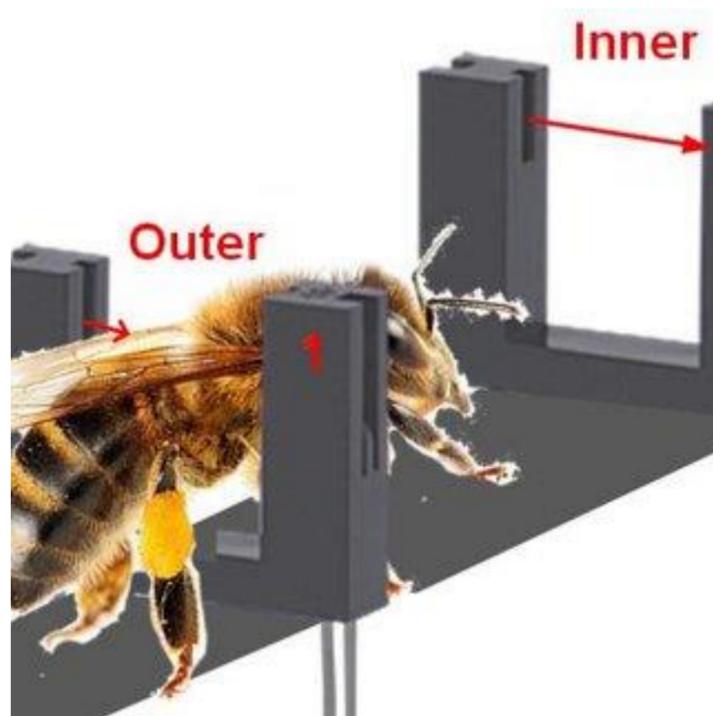
- Collaborate with bee's experts in the field of **Precision Apiculture**
- The audio sound produced by bees contains a lot of information about the colony state of health
- The goal is to enrich a new developed embedded system with possibility of detecting:
 - **swarming** events
 - **state of health** during winter when the beehive cannot be opened
 - **colony activity**
 - Etc...
- Characterize the power consumption of the system
- The aim is to validate the system in an experimental apiary



Bee Counter

Description:

- Develop a system to count the number of bees entering and exiting the beehive. Traditional methods utilize external cameras with machine learning algorithms for bee counting. However, camera-based systems are impractical in real scenarios due to their large size. Additionally, they consume a lot of power and require high computing resources. The goal is to collaborate with the University of Tuscia to develop a custom electronic system capable of counting bees and estimating their activity, which serves as a reliable indicator of the colony's health.

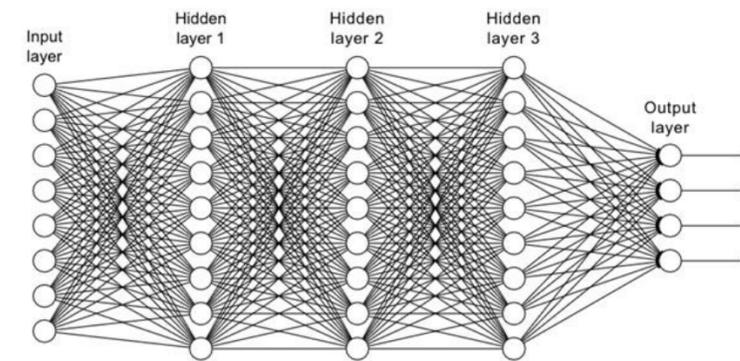
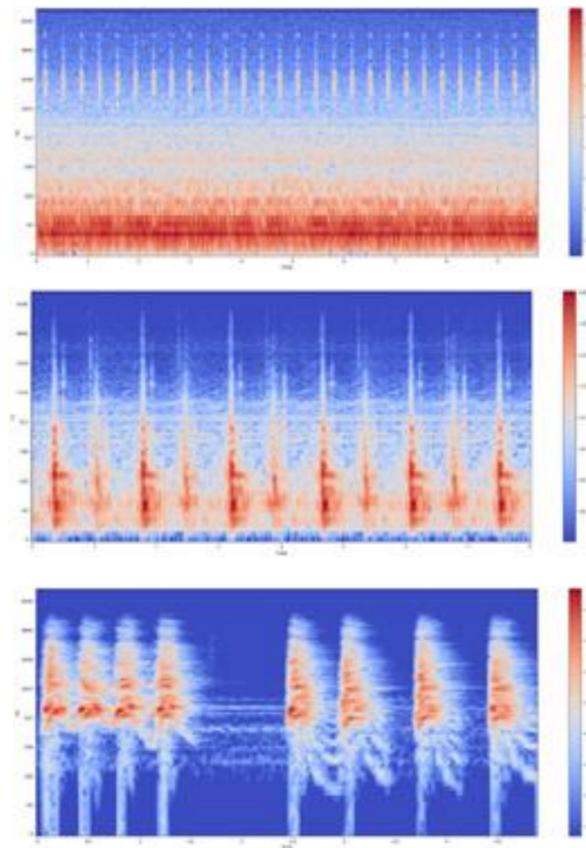


SOUND EVENT DETECTION & LOCALIZATION: Machine Learning and Beamforming



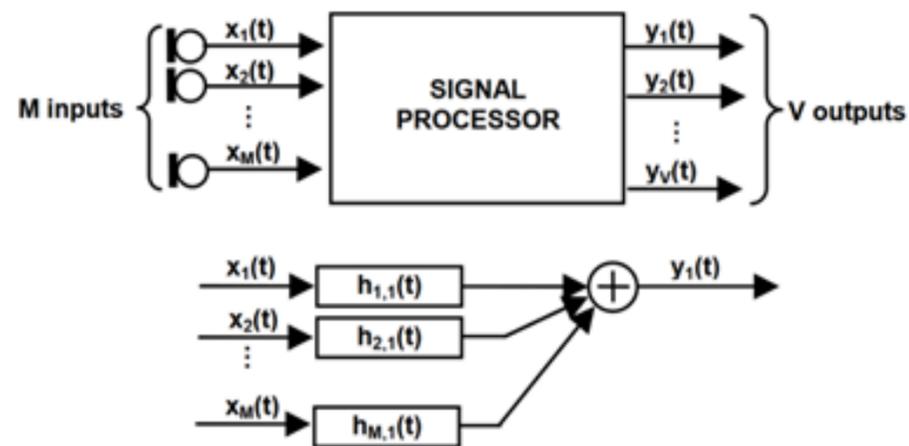
Machine Learning for Audio Applications

- In-vehicle sound detection
 - improvement of comfort
 - Improvement of safety
- Using only audio data
 - Signal processing (Noise Filtering, ...)
 - Feature extraction (Spectrograms, MFCC, ...)

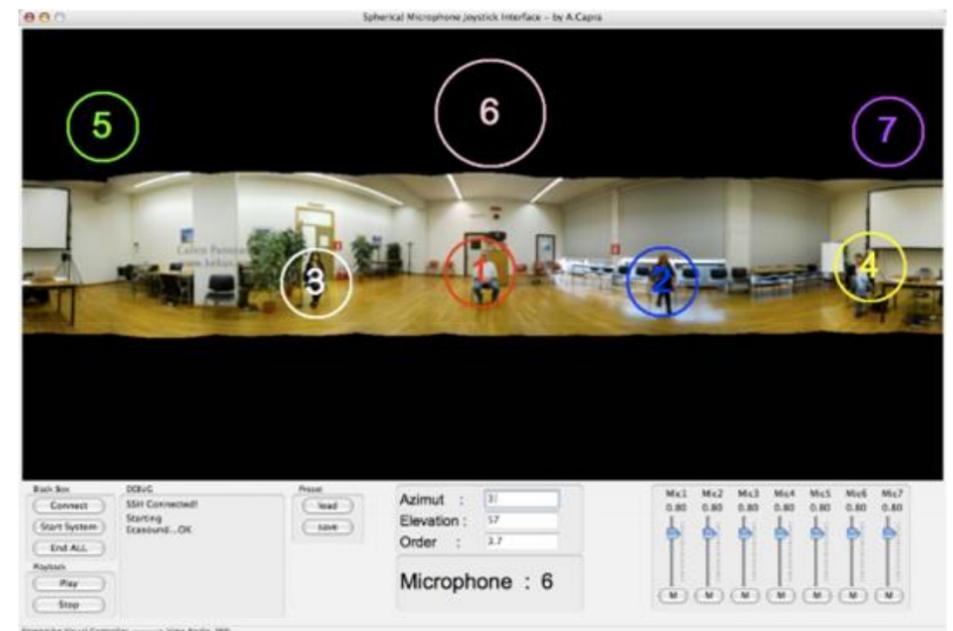


Beamforming for Direction of Arrival Estimation

- Provides the capability to distinguish different sound positions
- This technique allows to identify the sound position without using the video
- Use an array of omnidirectional microphones for creating virtual directive microphones
- Enhance sensitivity in the targeted direction improving the SNR

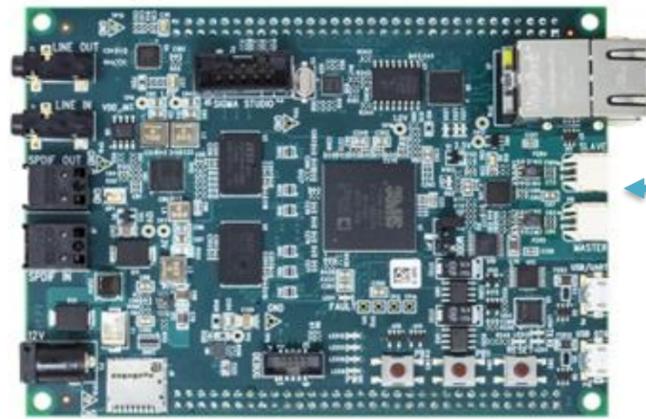


<https://youtu.be/XSplQWhluJE?feature=shared>



In-Car Sound Detection

Analog Devices SHARC Audio Module



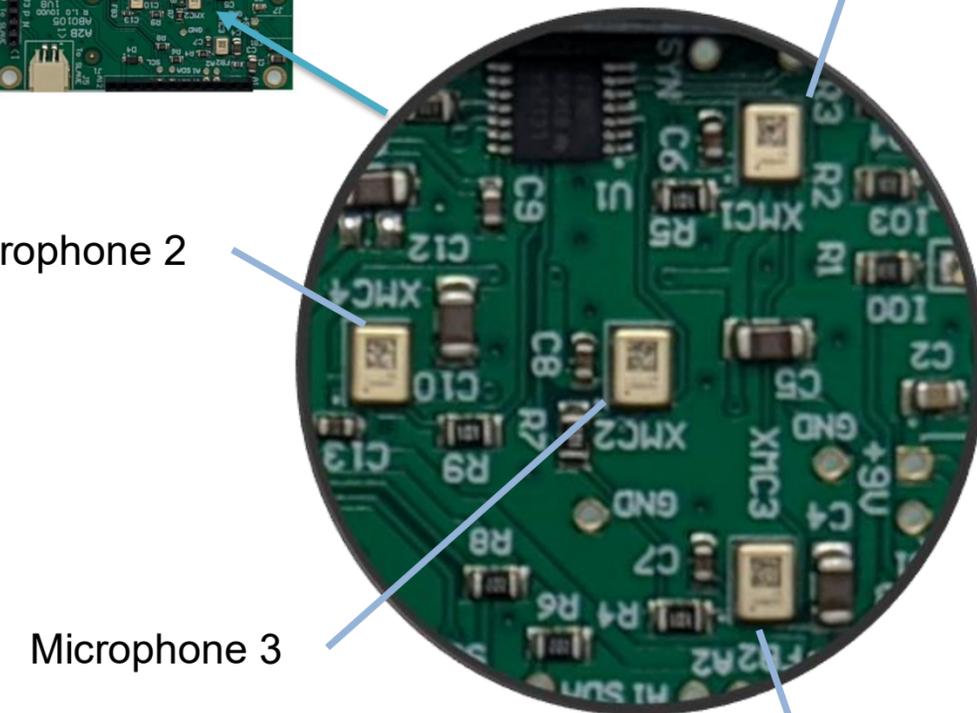
Automotive Audio Bus

CLOCKWORKS EVMA2B05



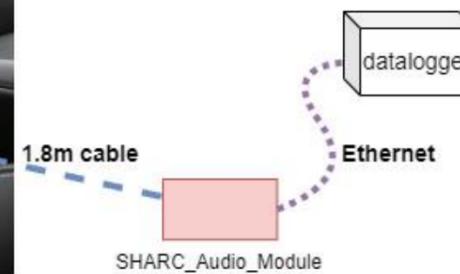
Microphone 1

Microphone 2



Microphone 3

Microphone 4



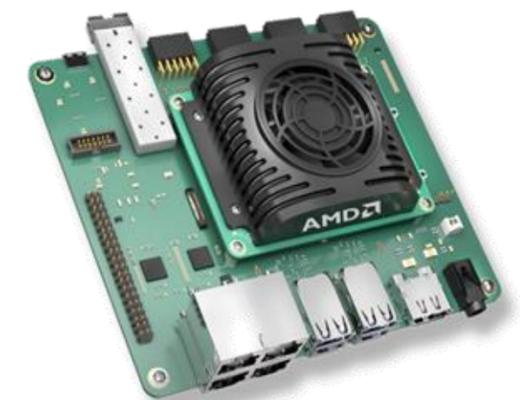
Acceleration of beamforming algorithms

- Description:
 - create a system capable of acquiring 64 microphones
 - conversion from Pulse Density Modulation (PDM) to Pulse Code Modulation (PCM)
 - signal processing in hardware (Filters, FFT, ...)
 - neural network implementation
 - time analysis and limits for real-time applications

- You will learn:
 - VHDL language for signal processing
 - Xilinx Design Flow methodology
 - Audio communication protocols
 - Git versioning tool



- Kria KR260**
- Zynq™ UltraScale+™ MPSoC EV (XCK26)
 - 256K system logic cells
 - x4 RJ45 Ethernet interface
 - x4 Pmod 12-pin interface (64 microphones)

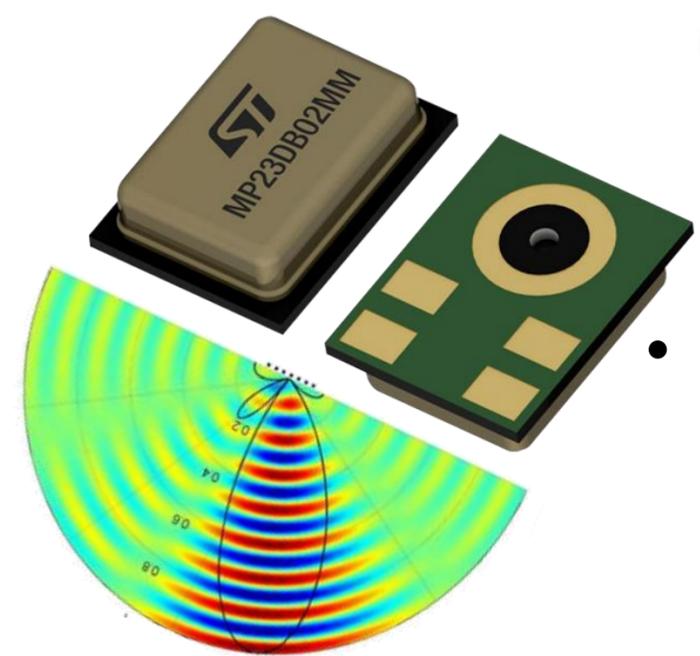
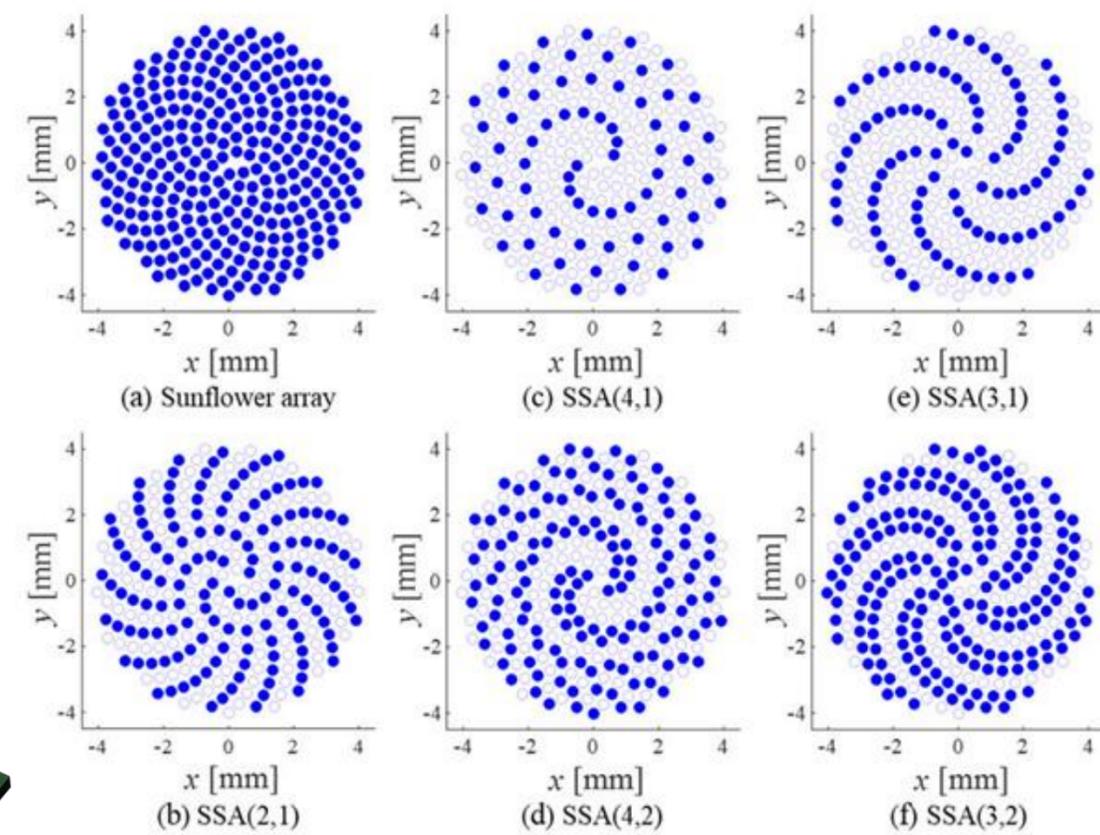
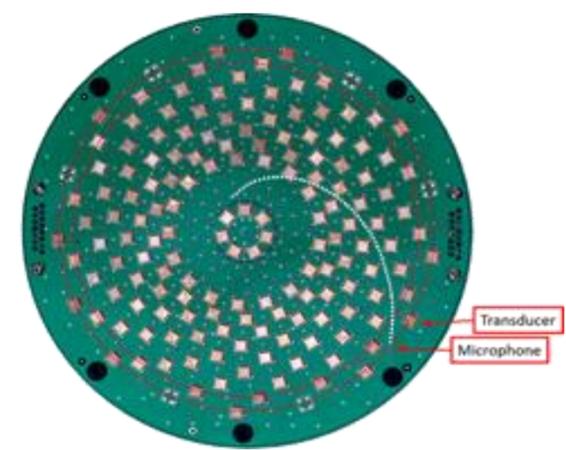


- STMicroelectronics**
- STEVAL-MIC001V1**
- ST MEMS microphone
 - PDM output signal
 - Clock speed 2MHz



Microphone array

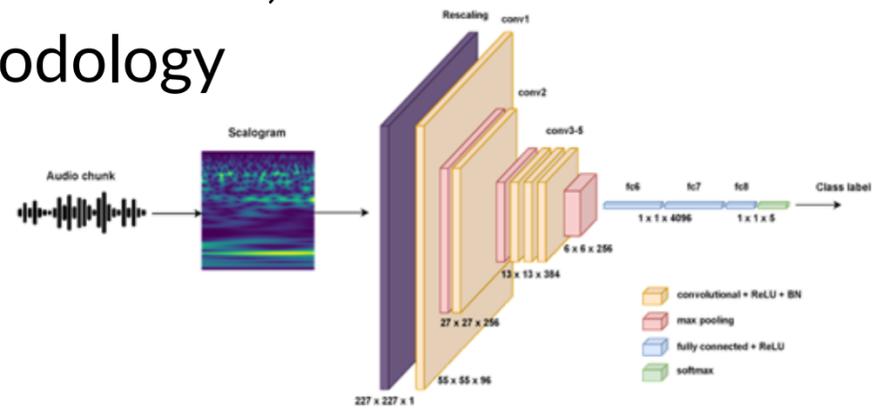
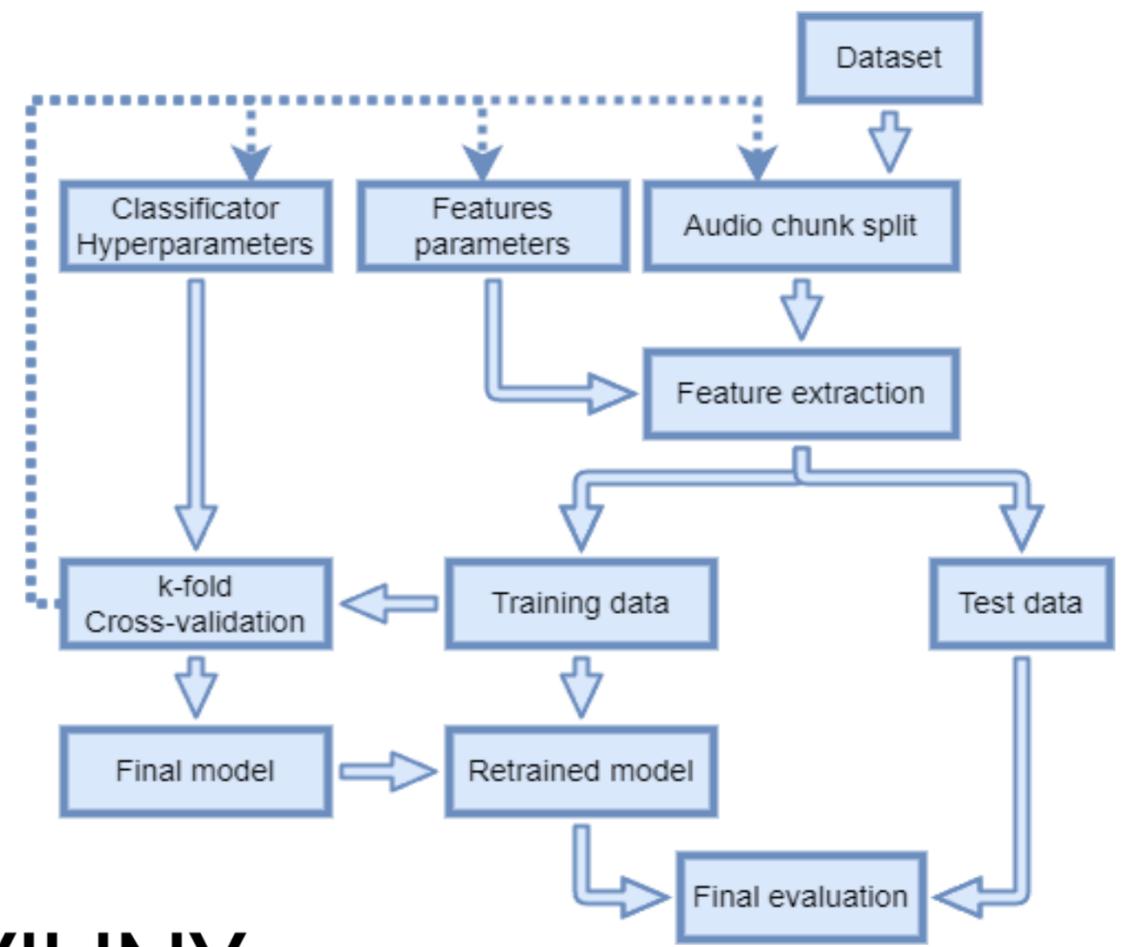
- Description:
 - PCB design with MEMS microphone array
 - reconfigurable array
 - characterization of microphones in anechoic chamber
 - Implementation of beamforming algorithms



- You will learn:
 - CAD tools for the design of PCBs
 - Python for beamforming algorithms

Design framework acoustic event detection

- Description:
 - Design framework for training neural networks
 - CNN network to be applied to spectrograms (images)
 - LSTM network for real-time classification
 - Acceleration of the training on GPU
 - Final implementation on FPGA
- You will learn:
 - Python and Git for the framework development
 - machine learning libraries: pytorch, scikit-learn, etc...
 - audio libraries: librosa, torchaudio, ...
 - Xilinx Design Flow methodology



BIOMEDICAL APPLICATIONS:

Enhanced Cardiovascular Health

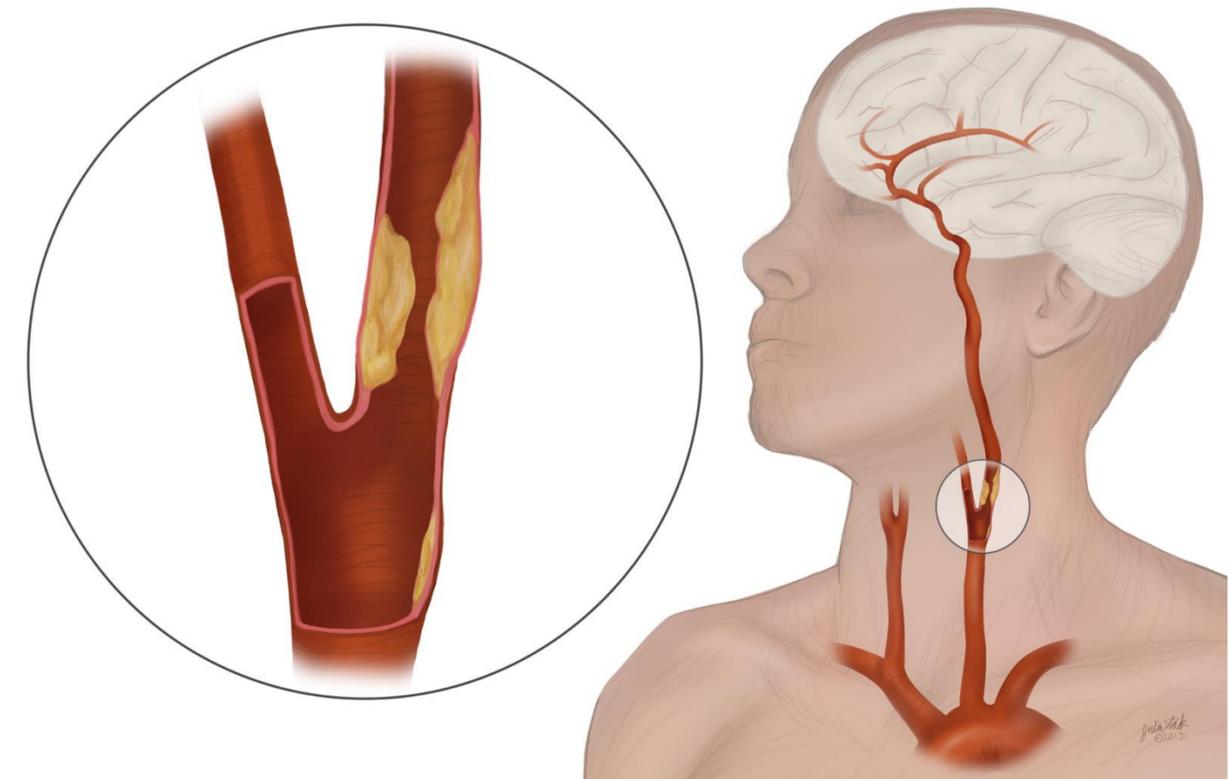
Brain Stroke Monitoring System

Alzheimer's disease early detection



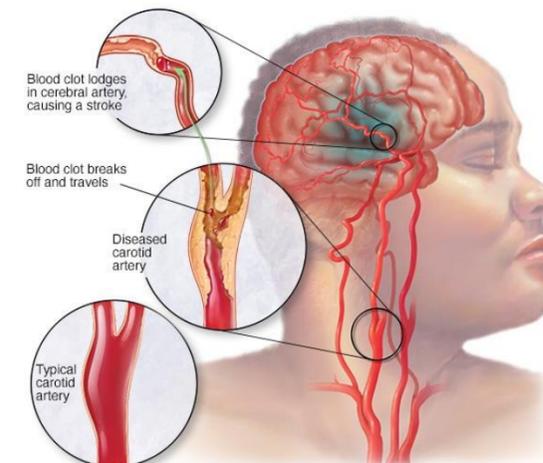
Carotid Artery Stenosis

- Monitoring **cardiovascular health** is essential given the widespread impact of cerebrovascular diseases
- The **carotid stenosis** is responsible for numerous deaths globally each year
- The significant **vessel narrowing** due to plaque buildup, severely restricting blood flow and increasing **stroke risk**
- Although effective, **traditional diagnostic methods** like ultrasound, magnetic resonance (MR) angiography, and computed tomography (CT) angiography are **limited by their need for advanced equipment and specialist expertise**



Carotid Artery Stenosis

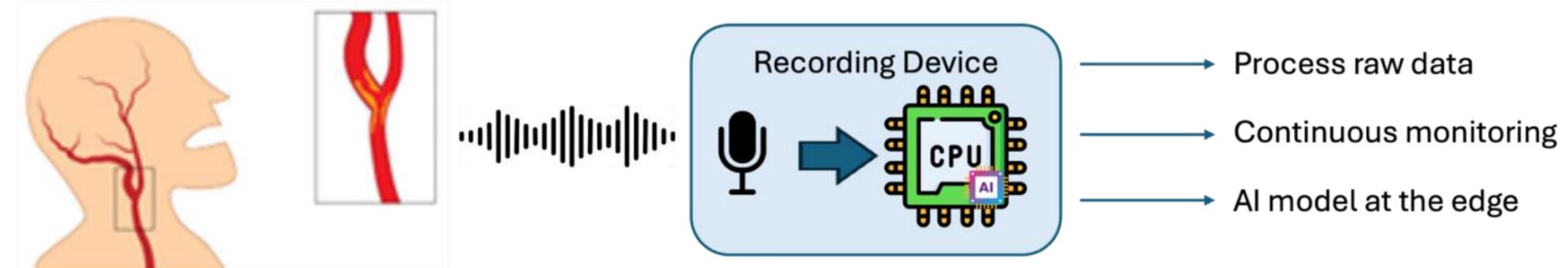
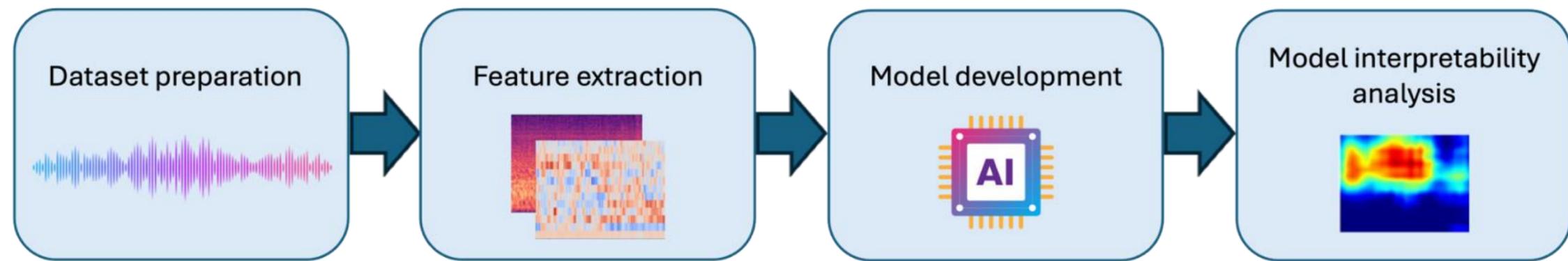
- **Phono angiography** uses a stethoscope to detect bruits and sounds caused by turbulent flow within arteries indicating potential stenosis
- This approach, often supplemented by computer-assisted auscultation tools, relies heavily on the clinician's experience
- The analysis of **heart sounds** is becoming an increasingly integral component of comprehensive cardiovascular risk assessment



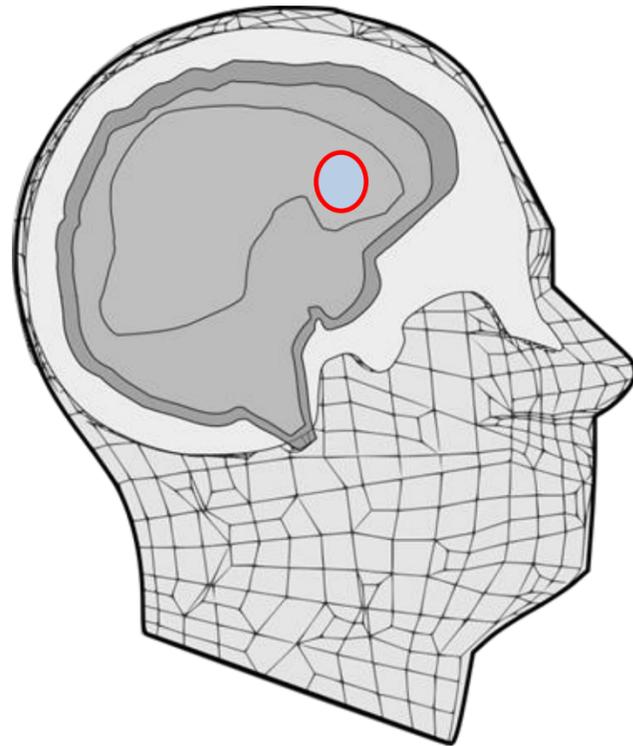
Carotid artery analysis

Description:

- Design of a custom, ultra-low power and portable electronic system
- Detect and analyze bruits (sound) produced by the carotid artery
- Acquisition of microphone audio
- Raw data processing
- Develop machine learning models that run at the edge for prediction
- Interface the system with PC through Bluetooth



Stroke Incidence



Someone has a stroke
every 2 SECONDS

Over 13M PEOPLE will have a stroke
each year



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#2

Stroke is the No.2 cause of
death behind heart disease.



1 IN 6 PEOPLE

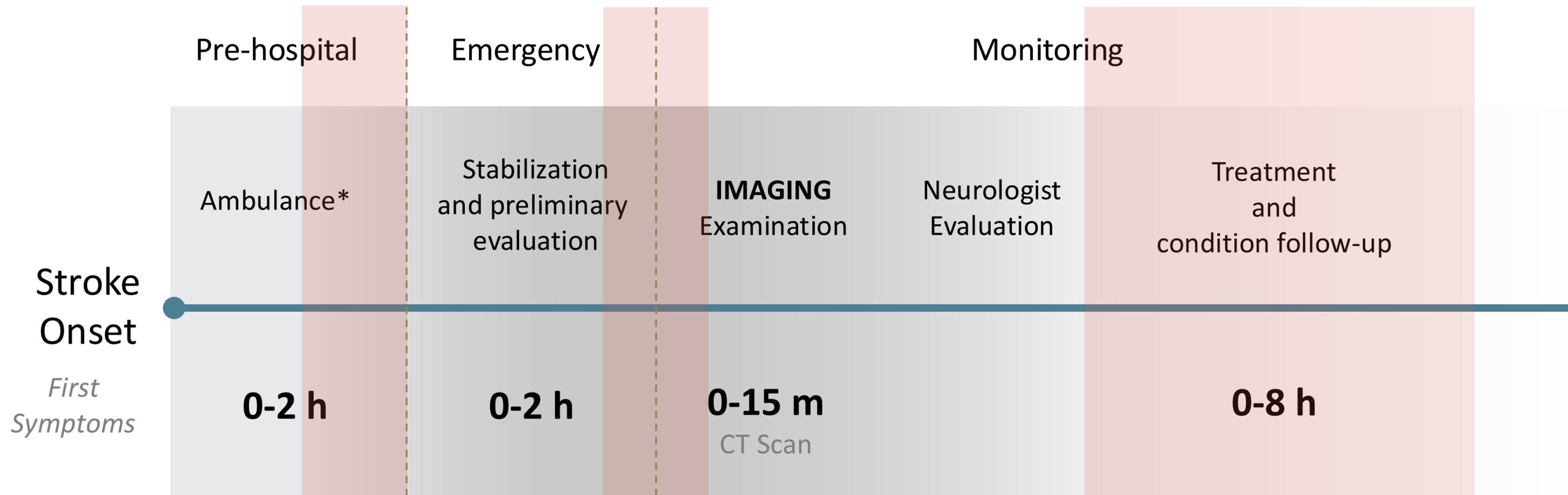
will have a stroke
in their lifetime.

33

MILLION PEOPLE WORLDWIDE

had a stroke in 2010.
Slightly more than half (16.9
million) were first strokes*.

Our solution: Microwave Imaging



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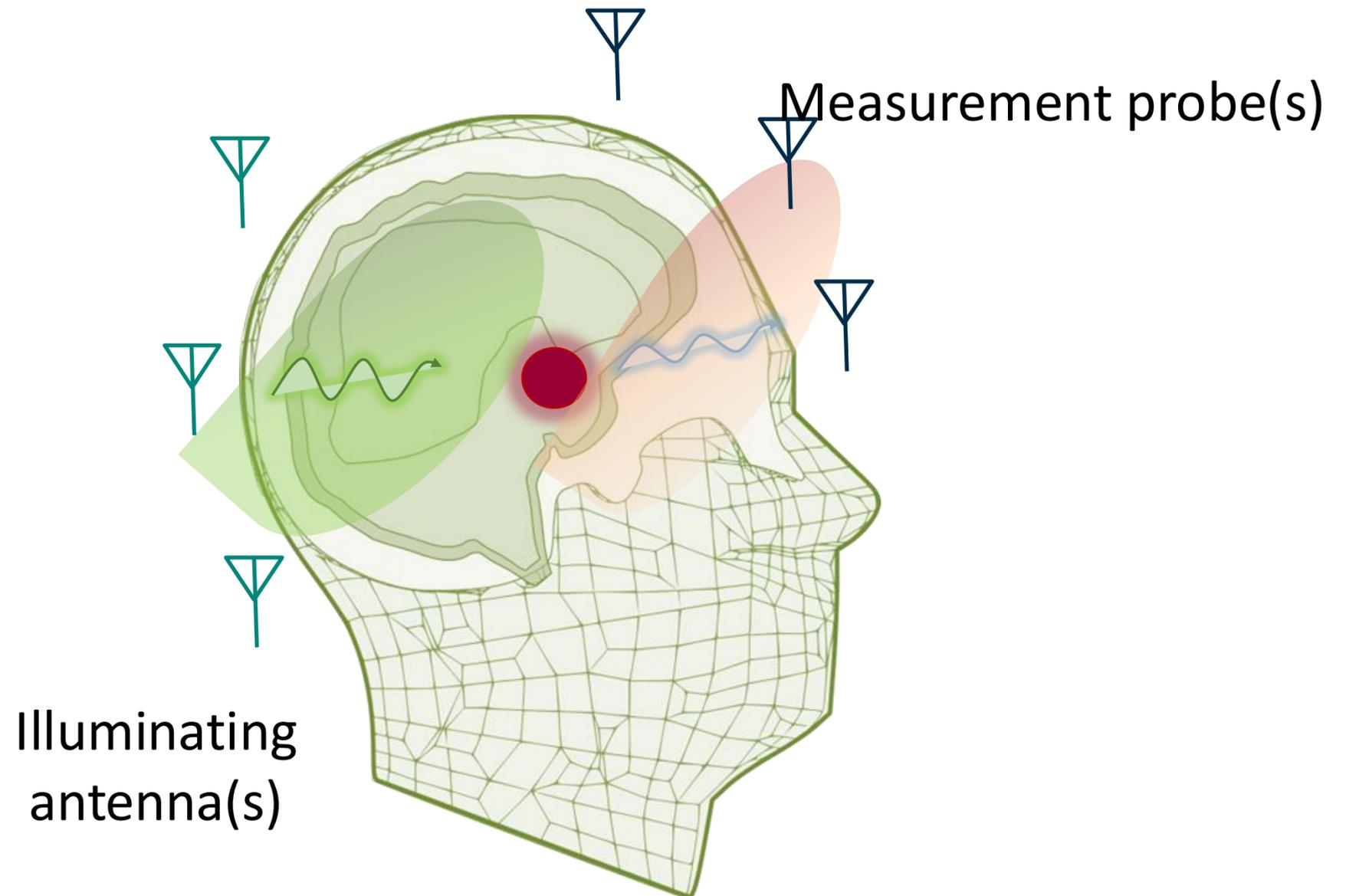
Giovanna Turvani



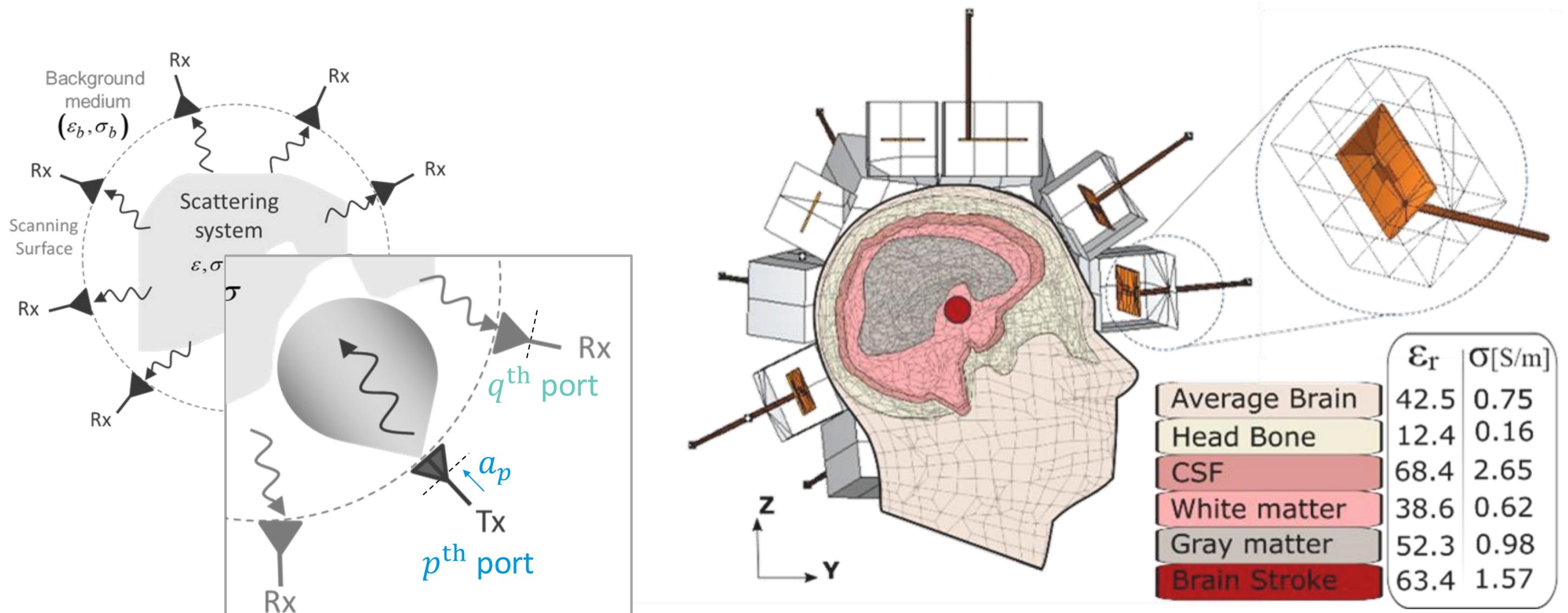
Principle



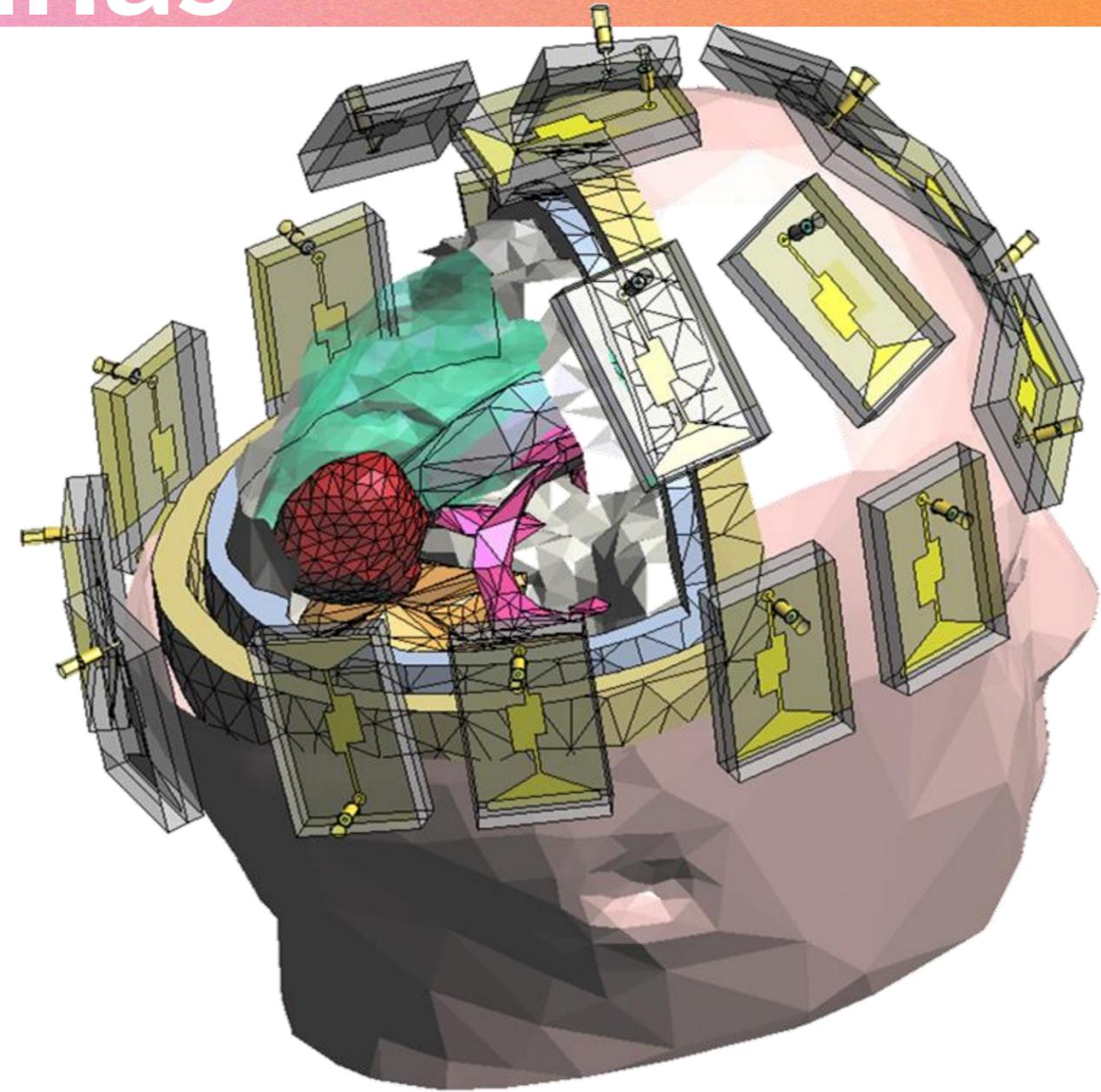
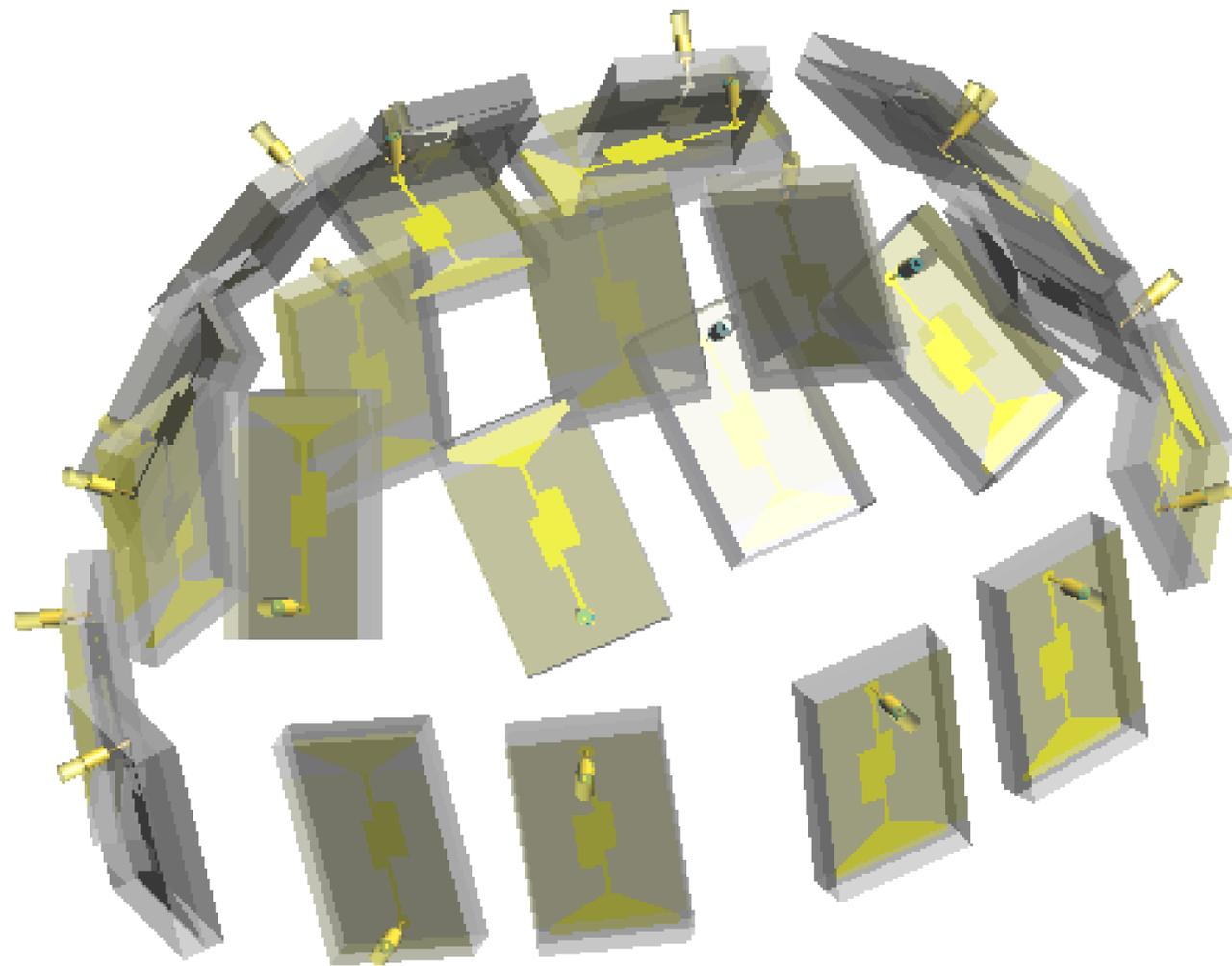
Electrical contrast
between the healthy
tissues and stroke
affected zones



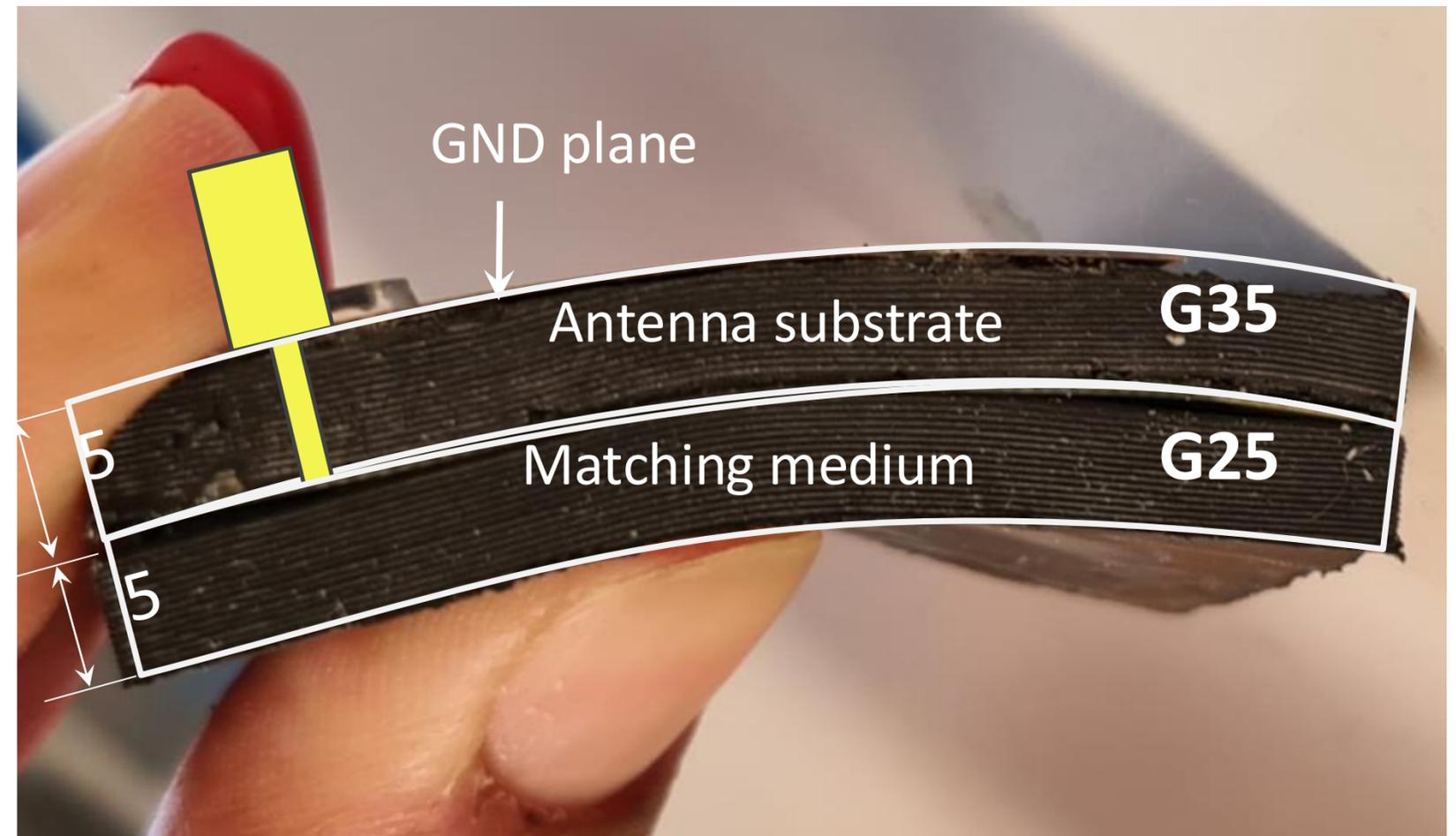
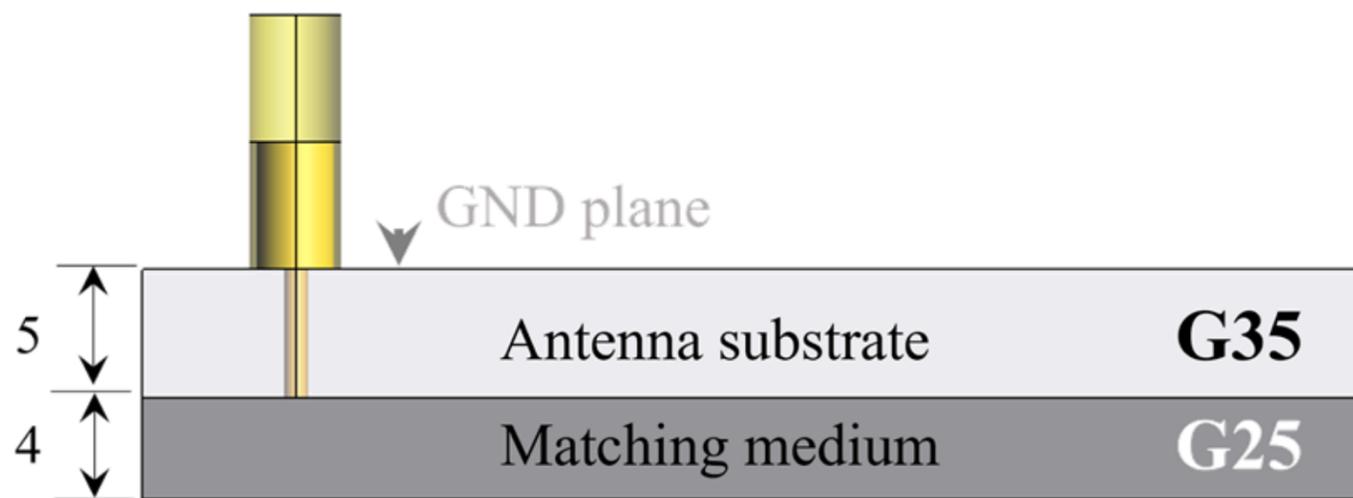
Step 1: build a Brain phantom



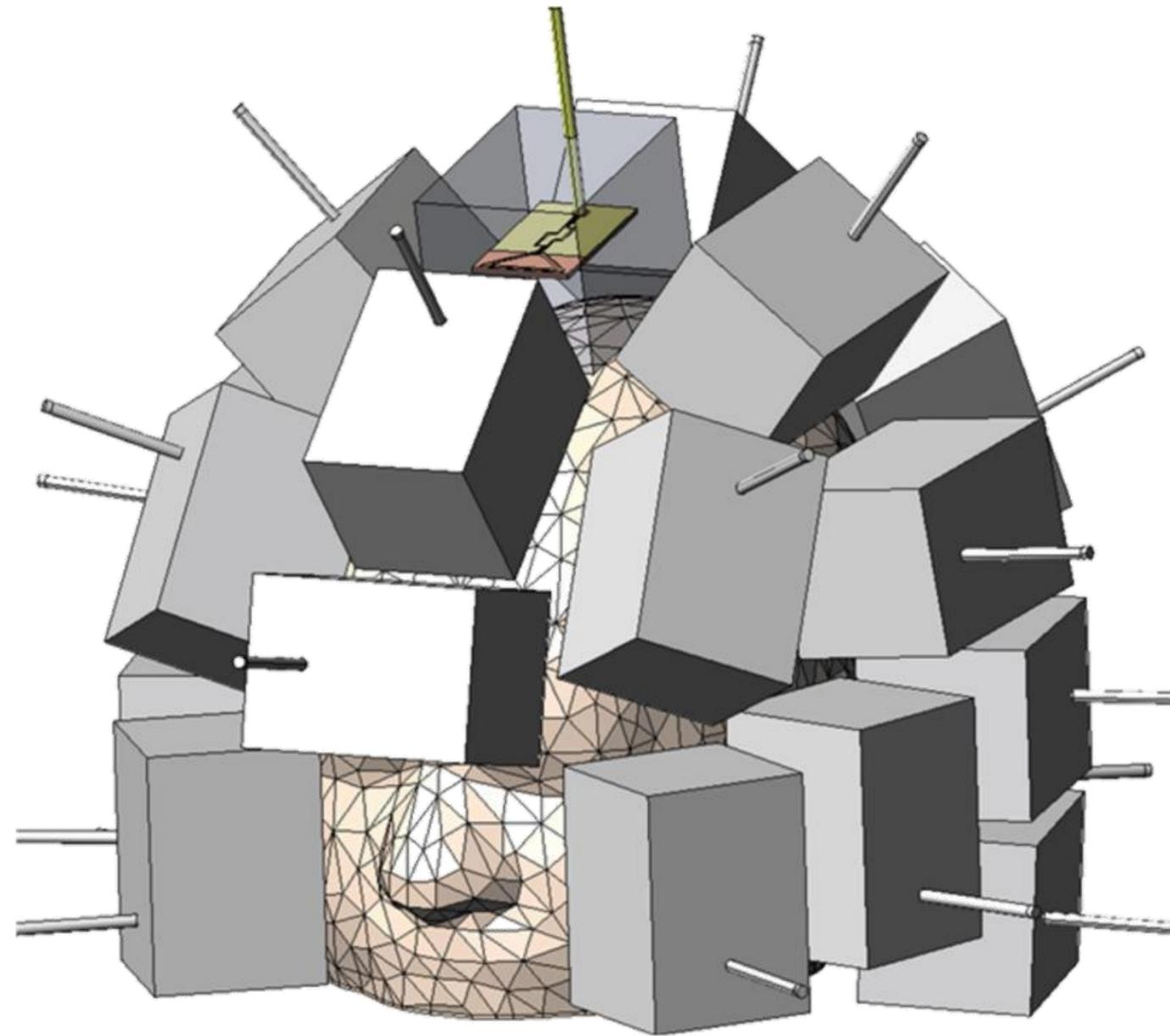
Step 2: build a model with 24 TR/RX antennas



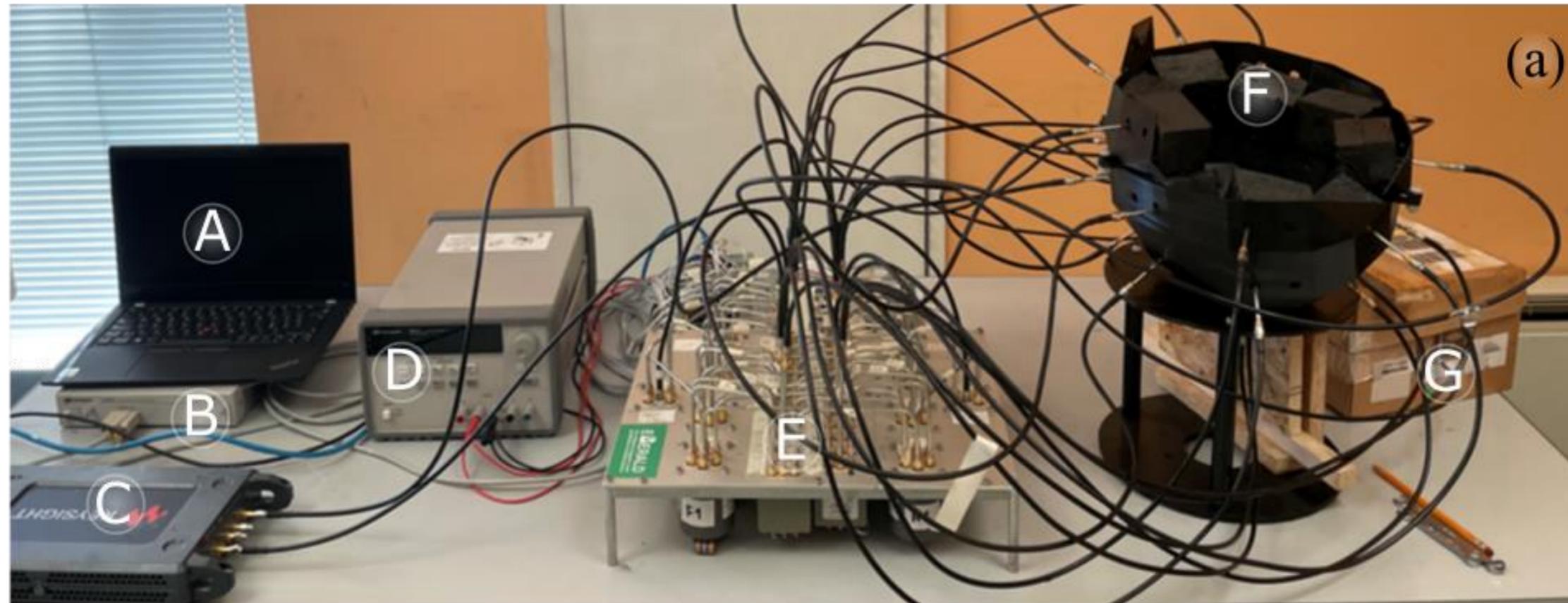
Matching medium



Prototype

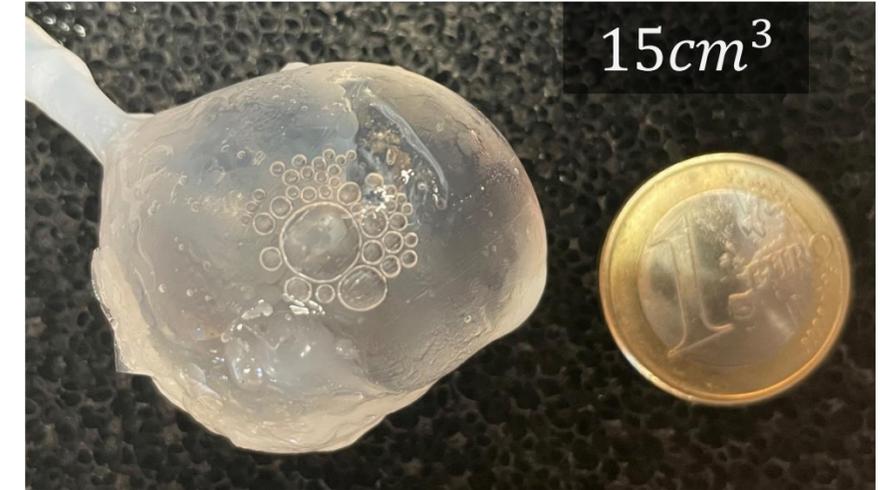
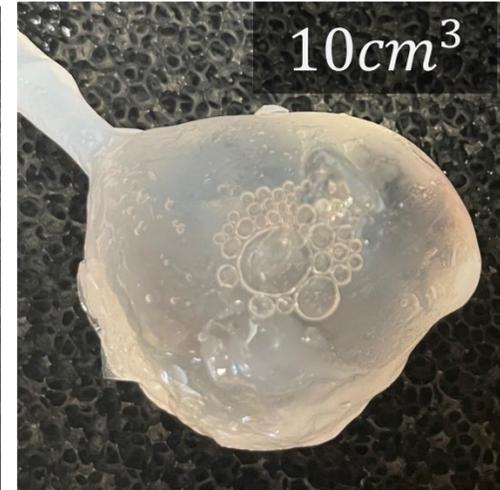


Experimental Setup



- Ⓐ Laptop
- Ⓑ Switch control
- Ⓒ VNA
- Ⓓ DC power source
- Ⓔ Switching matrix
- Ⓕ Brick antenna
- Ⓖ Reference channel
- Ⓗ Head phantom
- Ⓘ Average brain liquid

Numerical Validation: homogeneous head



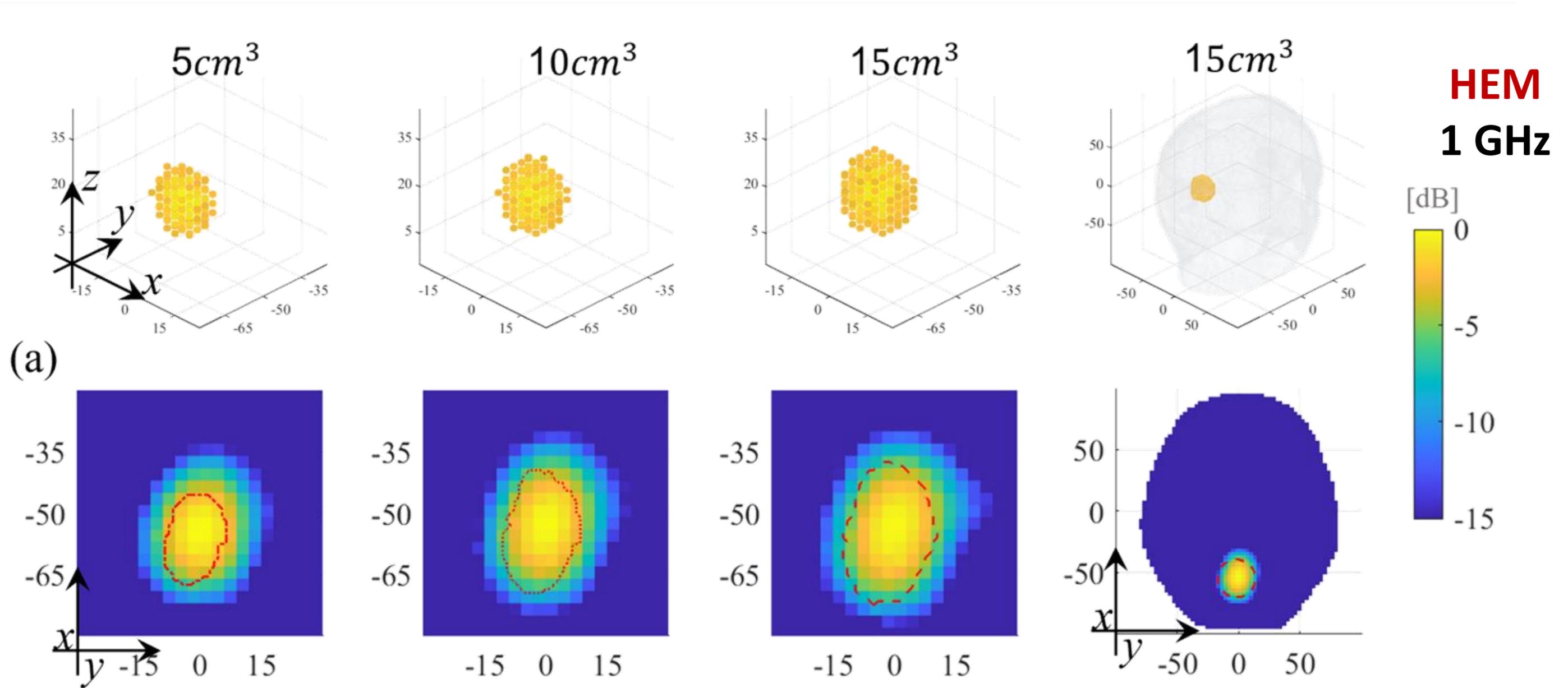
In collaboration with:



Giovanna Turvani

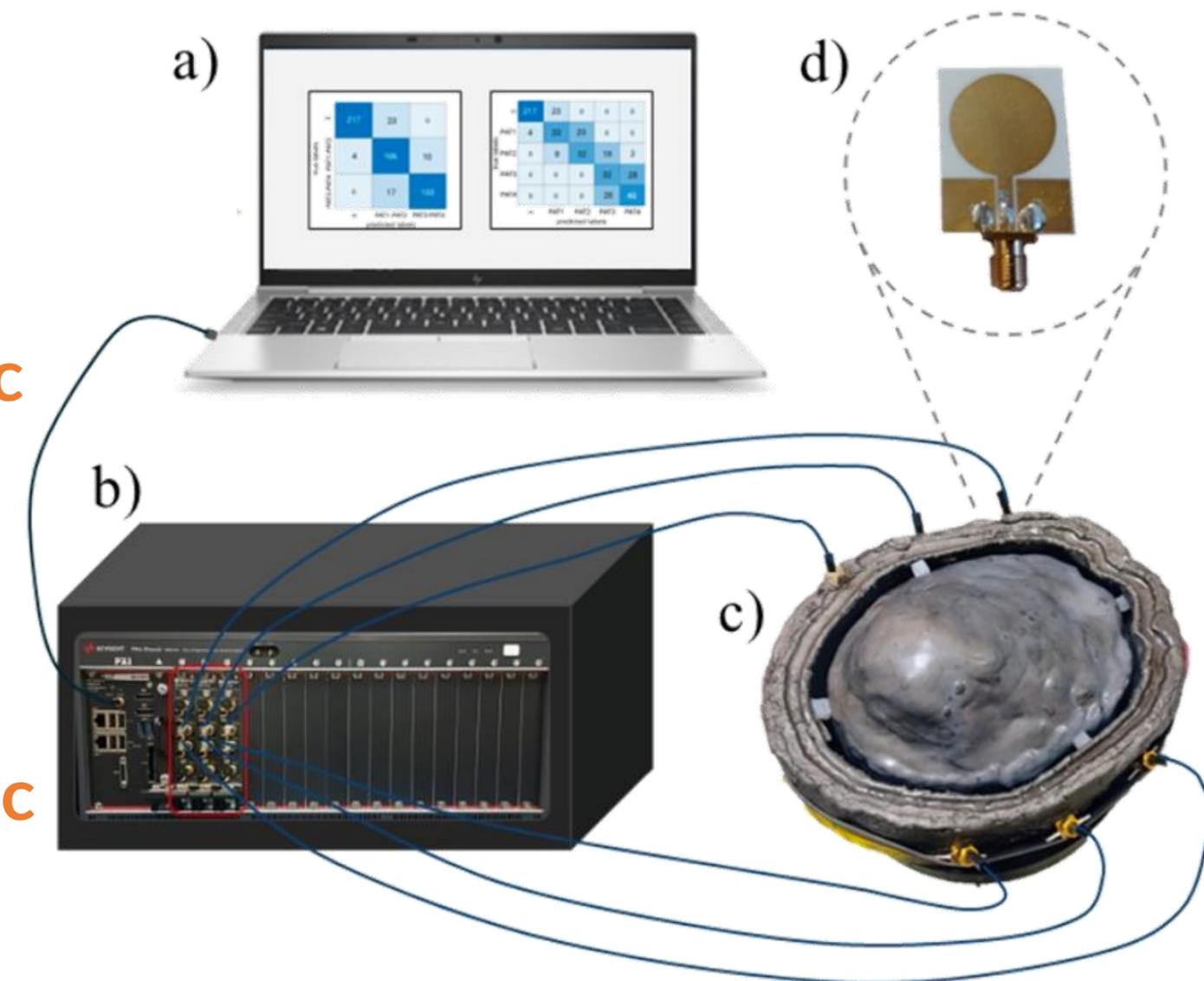


Numerical Validation: homogeneous head



Non-invasive microwave neuroimaging for enhanced Alzheimer's disease diagnosis

- ✓ Abnormally high accumulation of two proteins (amyloid-beta and tau) → **changes in Cerebral Spinal Fluid (CSF) dielectric properties**
 - Realization and experimental testing of a **microwave system for detecting CSF dielectric variations**
 - Development of CSF classification **algorithms** enhanced by **machine learning**
 - Realization and experimental testing of **realistic non-static multi-tissue head phantoms**



Tesi in collaborazione con



life.augmented



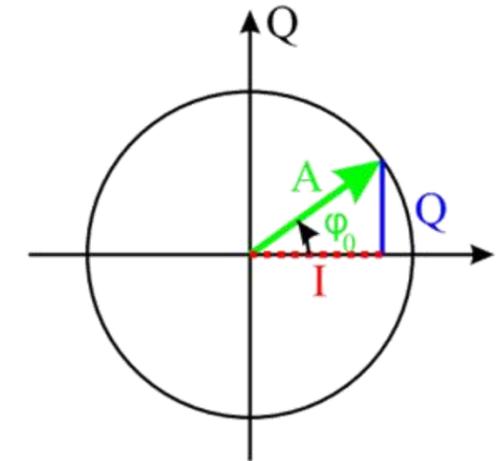
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IQ receivers

- A sine wave with phase ϕ can be always written as the sum of a sine wave and a cosine one, which are called **in-phase (I)** and **quadrature (Q)** components:

$$\begin{aligned} \sin(2\pi f_c t + \phi) &= \cos(\phi)\sin(2\pi f_c t) + \sin(\phi)\cos(2\pi f_c t) \\ &= I \cdot \sin(2\pi f_c t) + Q \cdot \cos(2\pi f_c t) \end{aligned}$$

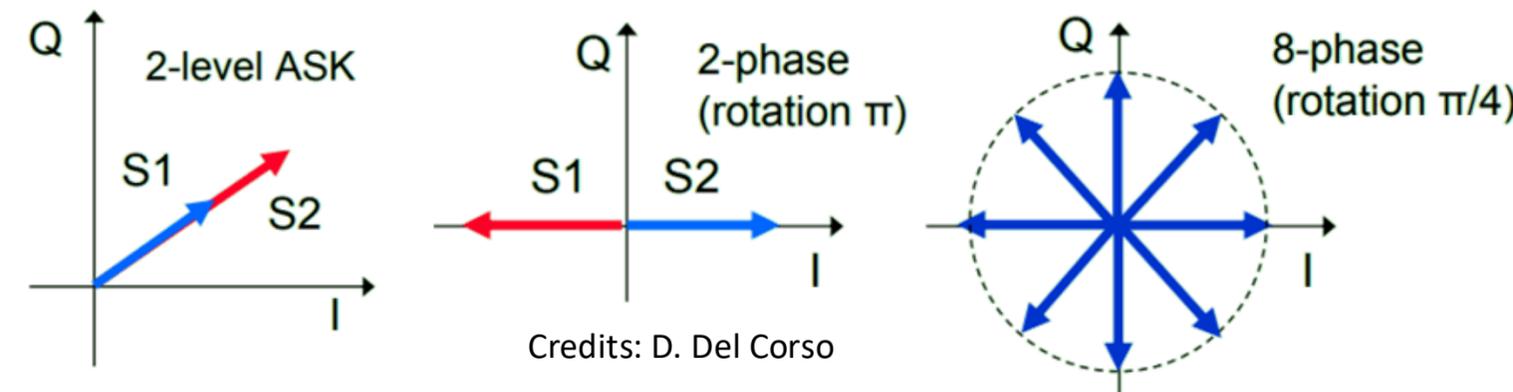
- An **IQ receiver** utilizes in-phase (I) and quadrature (Q) components to demodulate signals, enabling the extraction of amplitude and phase information from the received signal, with high spectral efficiency and improved signal-to-noise ratio (SNR).
- IQ receivers are widely used in various fields including telecommunications, radar systems, and medical imaging, providing precise and reliable signal processing capabilities.



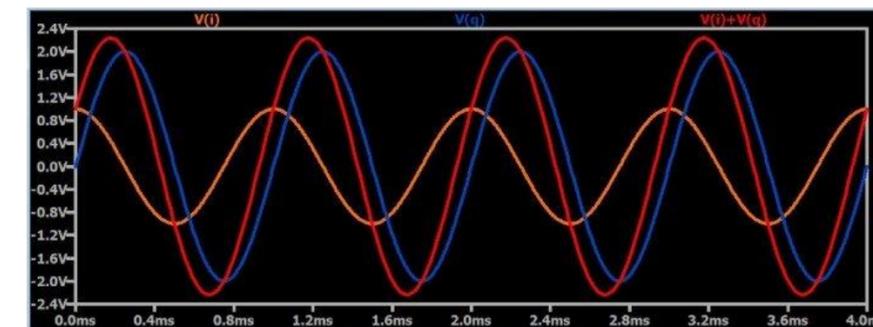
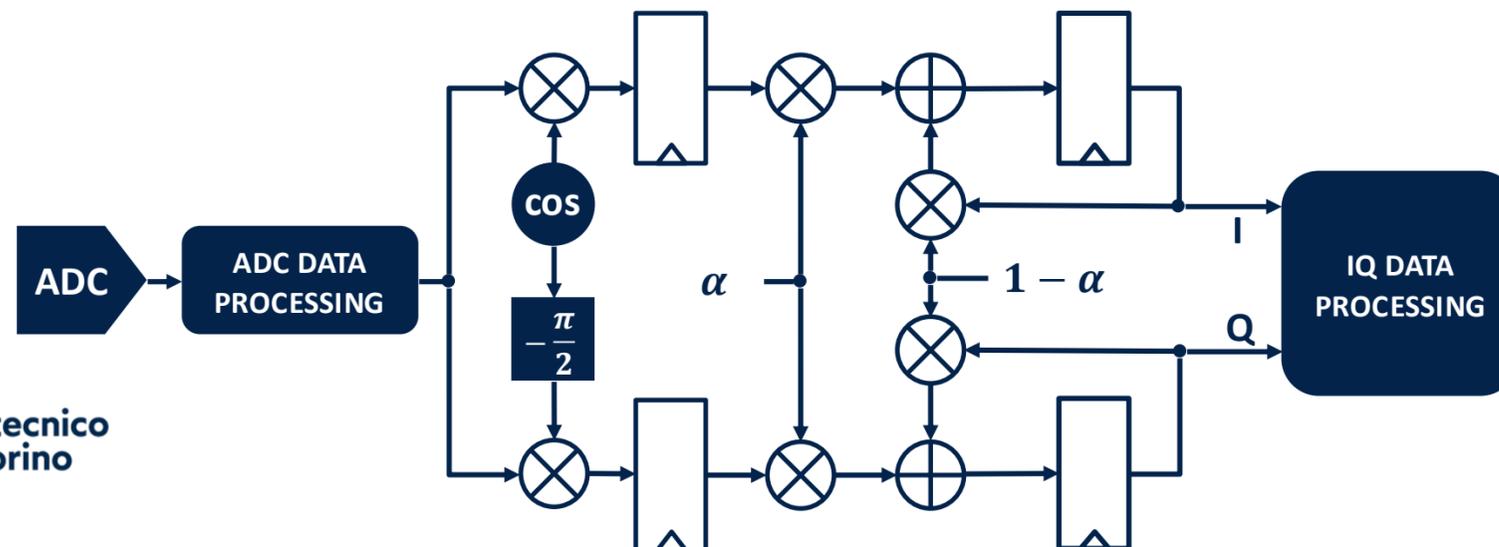
Schilcher, T. (2008). *RF applications in digital signal processing*.

$$\begin{aligned} I &= A \cdot \cos \varphi_0 & A &= \sqrt{I^2 + Q^2} \\ Q &= A \cdot \sin \varphi_0 & \varphi_0 &= \text{atan} \left(\frac{Q}{I} \right) \end{aligned}$$

Fig. 6: Phasor representation of RF signal



Credits: D. Del Corso

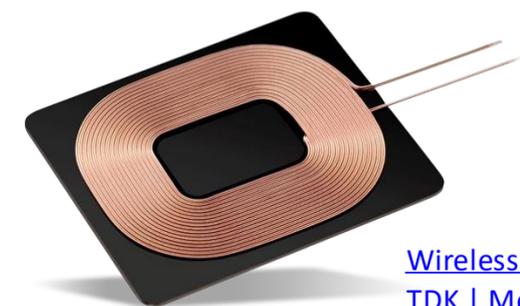


Wireless Power Transfer

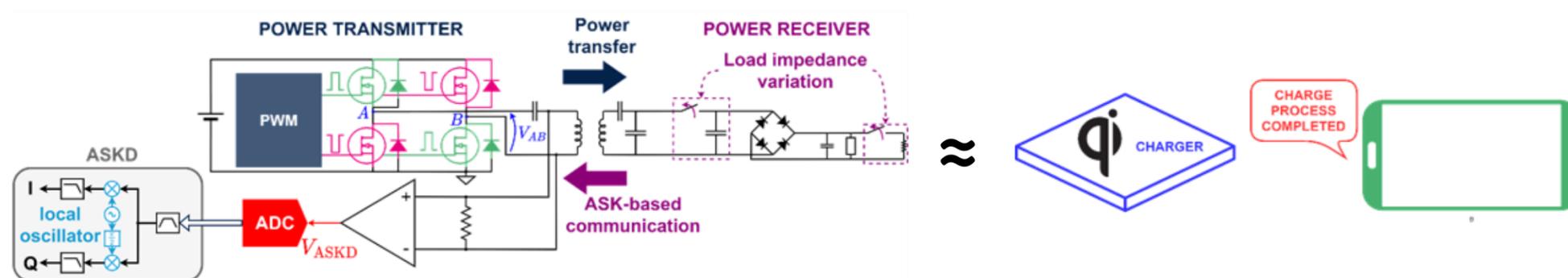
- **Inductive charging** is a technique for wireless power transfer from a power transmitter (PTx, i.e. the battery charger) to a power receiver (PRx, e.g. a smartphone or a sensor, etc.).
- Each terminal has a coil and mutual induction between coils, when put close to each other, allows the transfer of a *power signal*.
- The **Qi-standard** of Wireless Power Transfer consortium rules inductive charging.
- According to Qi standard, PRx communicates with PTx through **backscatter modulation**, which usually consists in an Amplitude Shift Keying (**ASK**) modulation of the current or voltage in the primary coil, through the variation of the load impedance at 2 kHz rate. This modulation is physically due to the mutual induction between coils.
- ST has already designed **full-digital ASK demodulators (ASKDs)**, integrated as peripheral in custom microcontrollers for wireless power transmitters.
- Magnetic Power Profile (MPP) is a WPT interface described in Qi 2.0, which can be considered a counterpart of Apple's Magsafe.
- Thanks to the presence of a permanent magnet, the device receiving power can stay in a more convenient position over the case, thus improving power delivery (up to 15 W).



[How to Choose the Right Wireless Charging Pad for iPhone or Android \(businessinsider.com\)](https://www.businessinsider.com)

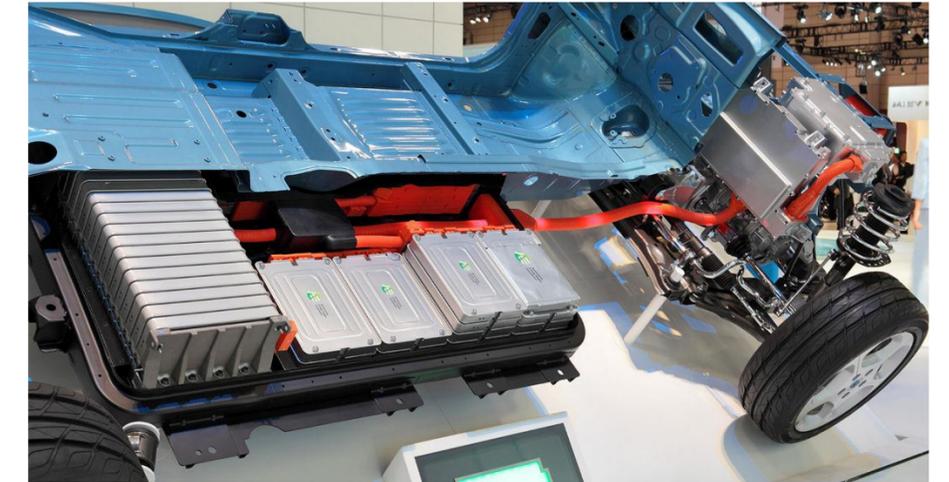


[Wireless Charging Coils - TDK | Mouser](#)



Electrochemical Impedance Spectroscopy

- The electrochemical impedance spectroscopy (**EIS**) provides a unique tool for the analysis of **the behavior of batteries** (e.g. of electric vehicles).
- Performing EIS on a battery does not significantly affect its status and the performance of the overall system (**non-destructive** technique).
- EIS can be performed *in operando*.
- EIS can be applied to full cell, half cells or individual cell components.
- **IQ** receivers can be exploited to compute **phasors** of voltage and current, whose ratio gives the impedance.



$$Z = \frac{V}{I}$$

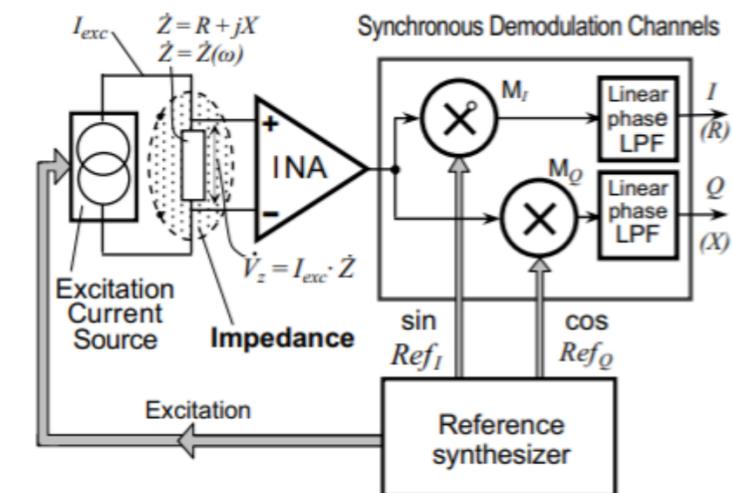
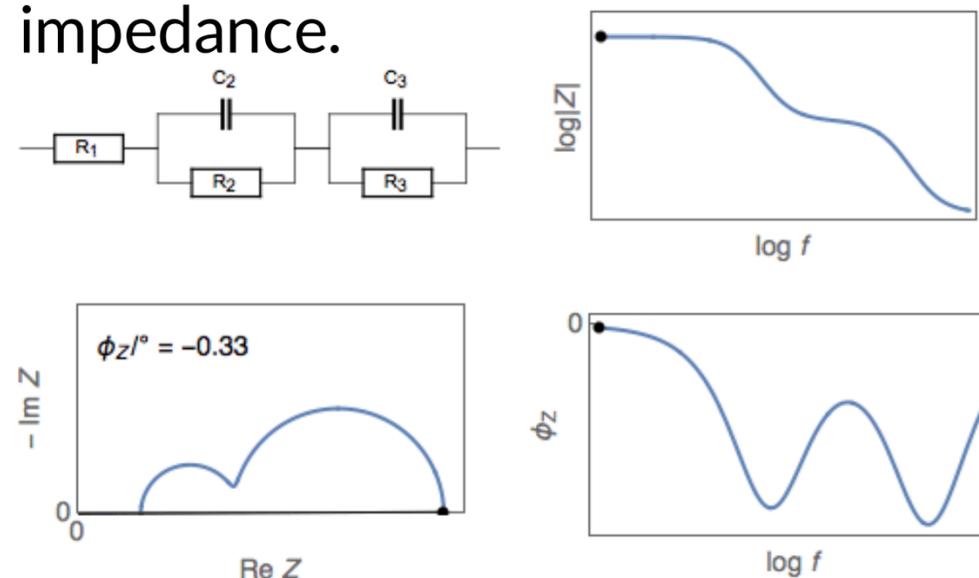
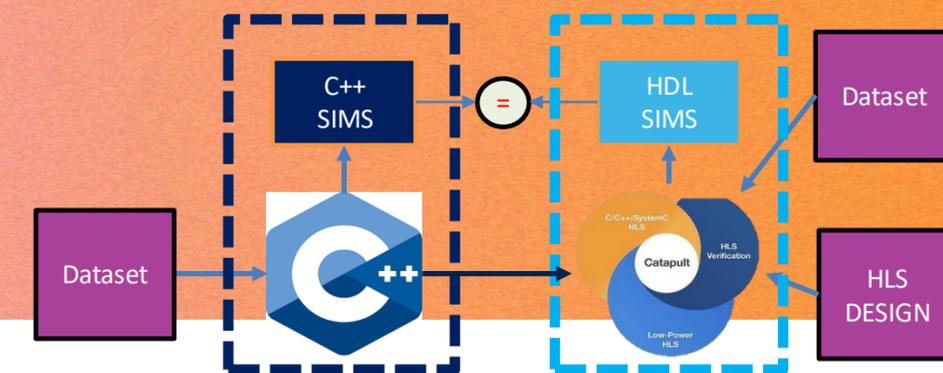


Figure 3. Signal processing in the impedance analyzer.

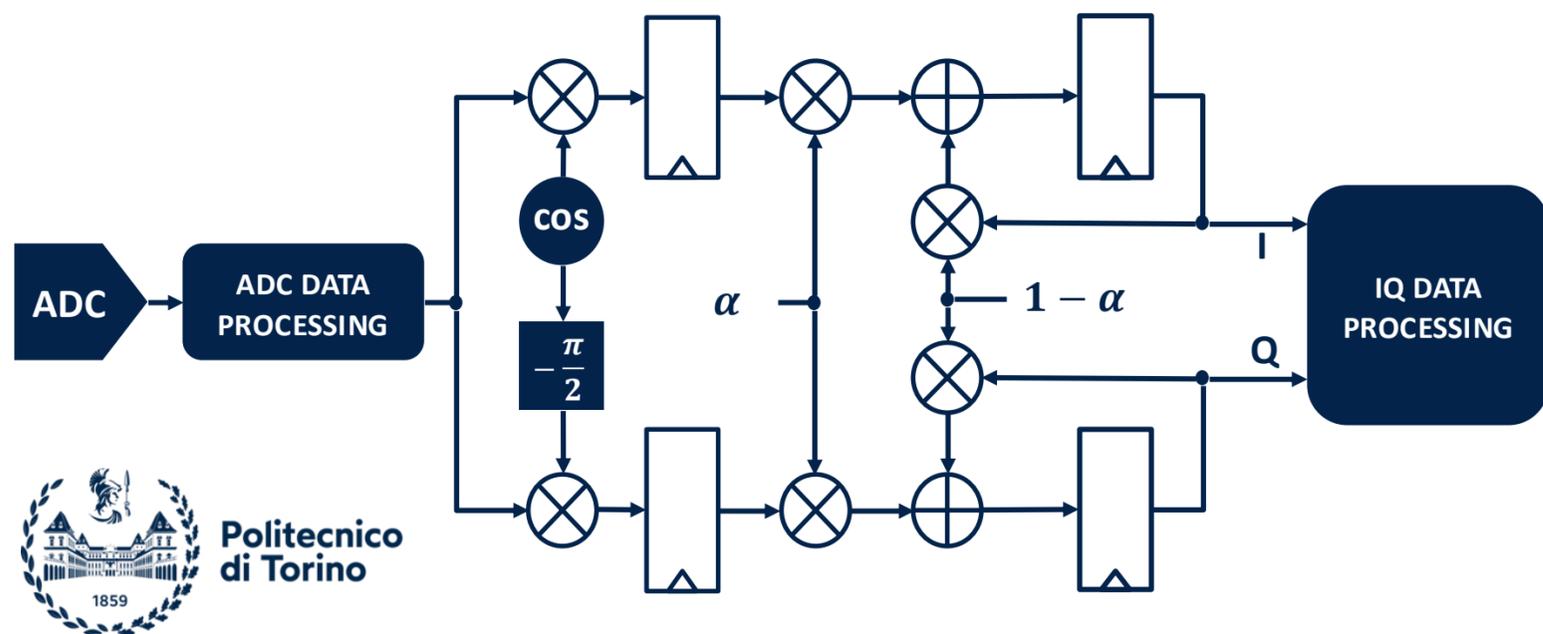
M. Min, "Embedded Signal Processing in Impedance Spectroscopy," 2008 NORCHIP, Tallinn, Estonia, 2008, pp. 47-52, doi: [10.1109/NORCHIP.2008.4738268](https://doi.org/10.1109/NORCHIP.2008.4738268)



- The APMS Central R&D team of STMicroelectronics is proposing a MSc thesis concerning the design of a digital IQ architecture, to be integrated in chips for:
 - wireless power transfer systems;
 - Battery Management Systems (EIS).
- Hardware design can be done at both canonical Register-Transfer Level (RTL) or with High-Level Synthesis (HLS) tools.
- HLS could simplify the design space exploration and the hardware generation, starting from a software model in C/C++. For this reason, the student could work on the definition of a robust design methodology for software-to-hardware design.
- The student will interact with ST engineers located in Cornaredo (MI) and Torino sites.
- DSP (and eventually HLS) knowledge is not mandatory. Industrial tutors will provide the required learning material.

Thesis workflow:

1. Definition of the DSP architecture (MATLAB/Python) depending on requirements.
2. Software/firmware implementation and validation with available datasets (C/C++).
3. Hardware digital design, done in RTL (SystemVerilog, Verilog or VHDL) or HLS.
4. Hardware validation.



QUANTUM COMPUTING:

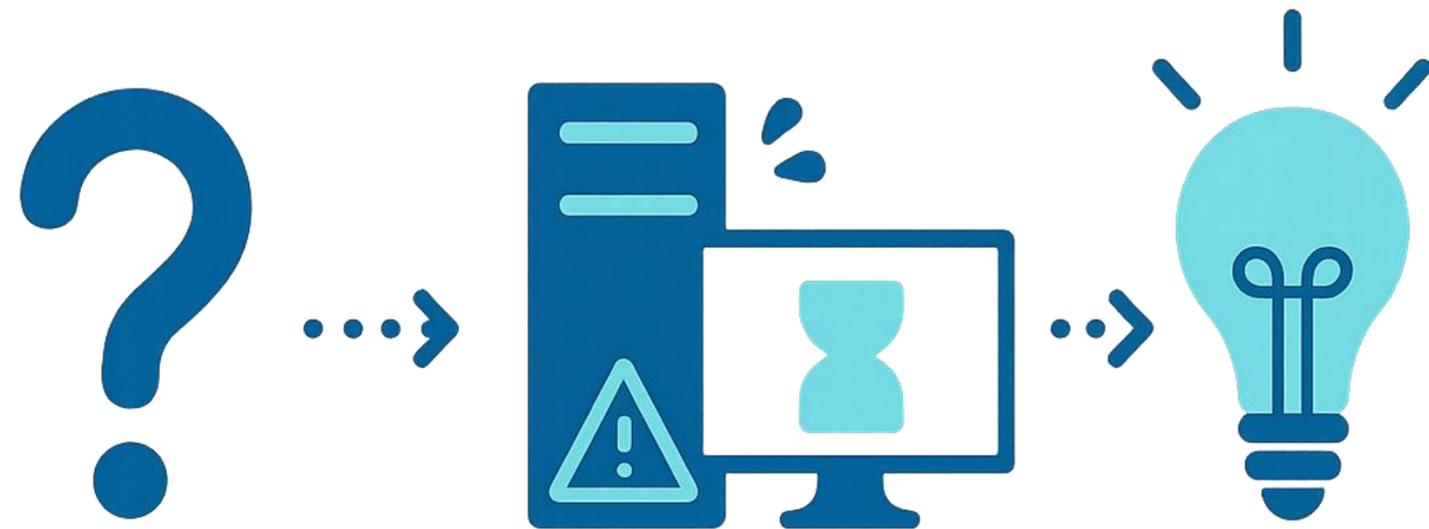
A short introduction



Politecnico
di Torino

Perché parlare di quantum computing oggi

- Viviamo in un mondo pieno di dati e problemi complessi da risolvere
- Alcuni problemi sono troppo grandi anche per i supercomputer tradizionali
- Il quantum computing è un nuovo approccio al calcolo, basato sulla meccanica quantistica



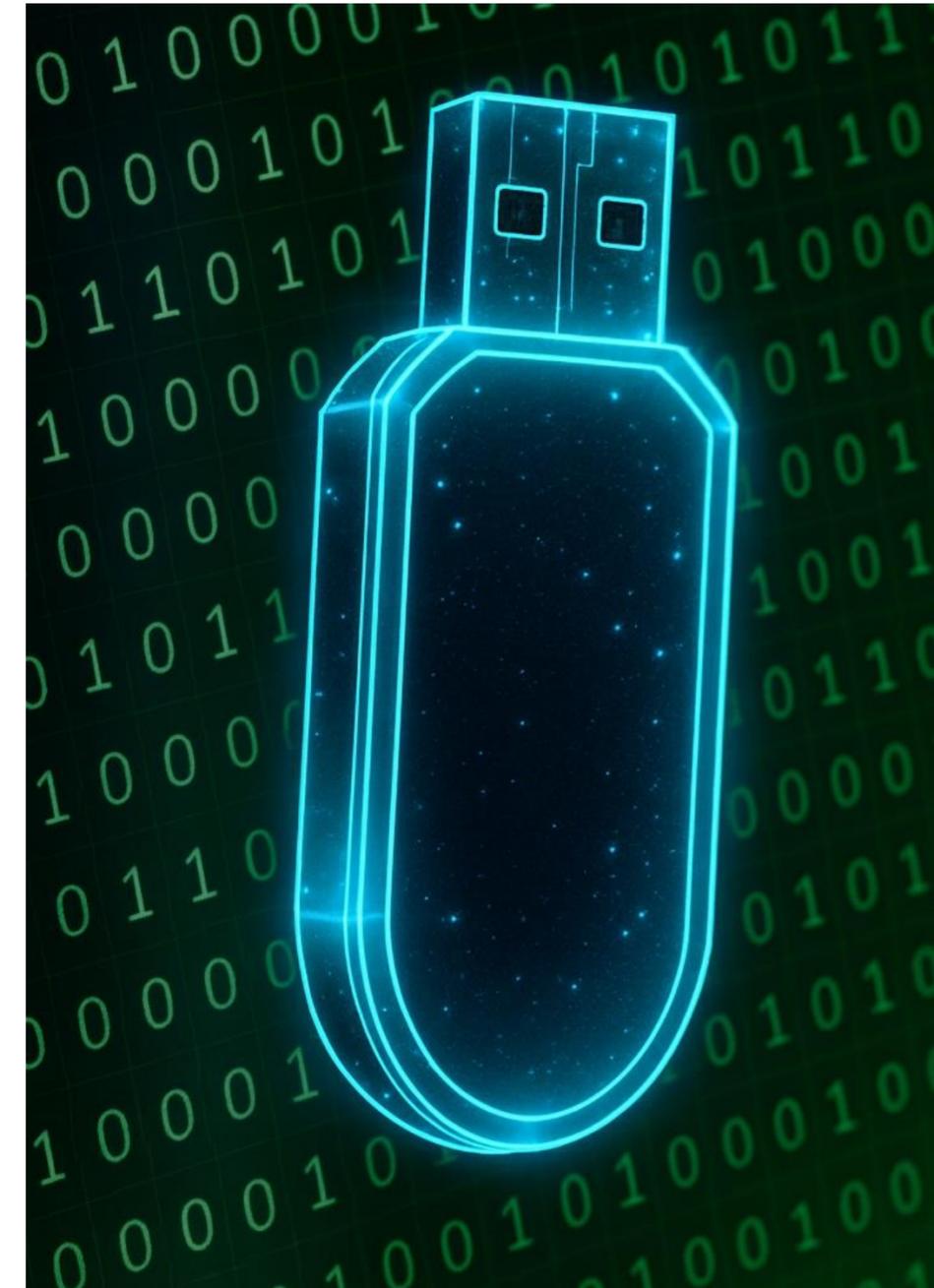
Che cos'è un computer classico



- È il tipo di computer che usiamo ogni giorno: PC, smartphone, server, tablet
- Funziona con circuiti elettronici e transistor che elaborano segnali elettrici
- L'informazione è rappresentata tramite bit, che possono valere solo 0 oppure 1

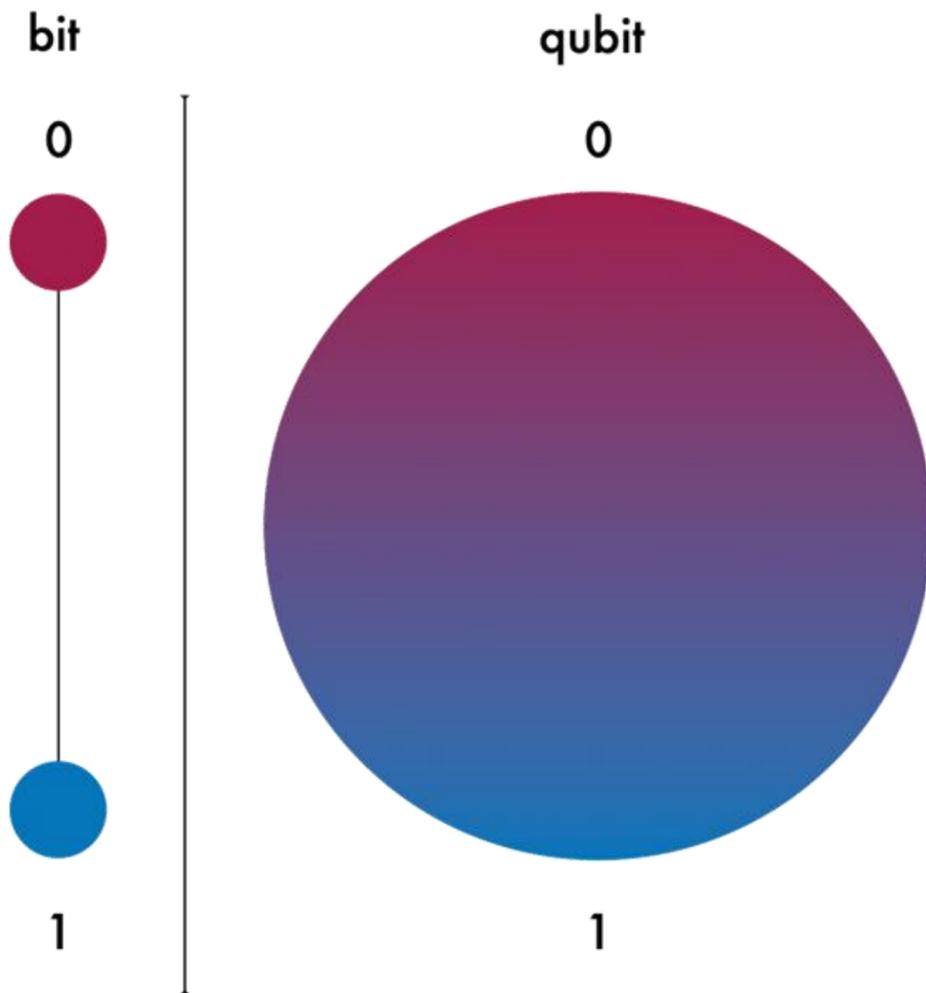
Il bit: unità base dell'informazione classica

- Un bit è la più piccola quantità di informazione in informatica
- Può assumere due stati possibili: 0 oppure 1
- Tutti i file (testi, immagini, video) sono alla fine sequenze lunghissime di bit



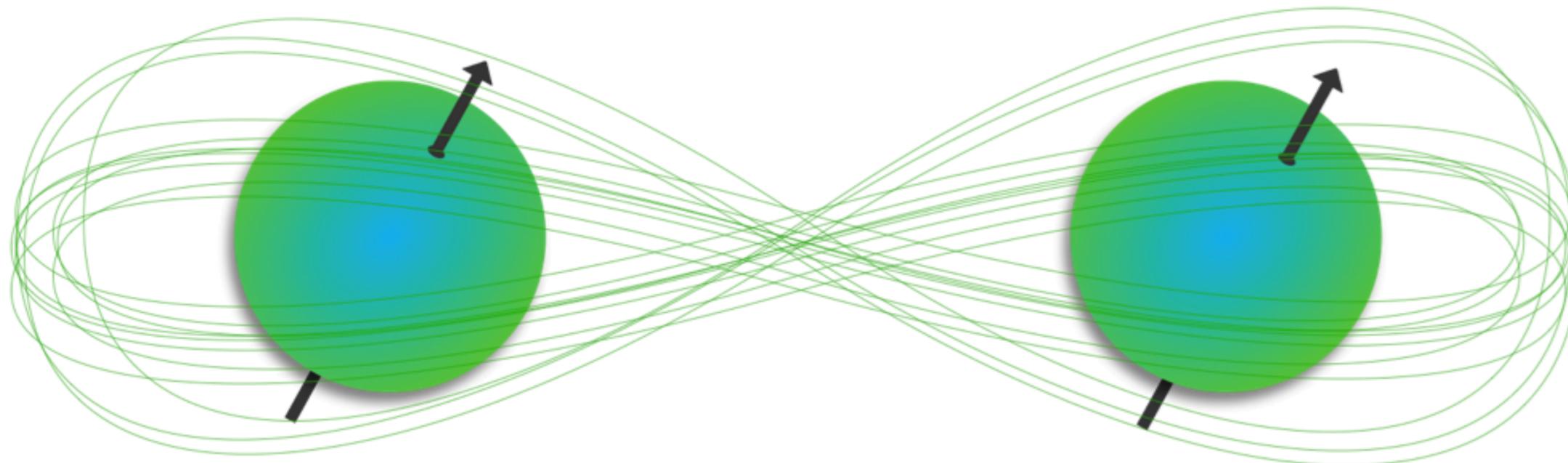
Sovrapposizione: 0 e 1 allo stesso tempo

- Nel quantum computing l'unità base di informazione è il qubit (quantum bit)
- Un qubit è realizzato con sistemi fisici quantistici, ad esempio spin di elettroni o fotoni
- A differenza del bit classico, il qubit sfrutta le leggi della meccanica quantistica
- Un qubit può trovarsi in sovrapposizione di stati: una combinazione di 0 e 1
- Finché non misuriamo il qubit, non è solo 0 o solo 1, ma una sovrapposizione dei due
- Analogia: una moneta che gira in aria non è ancora solo testa o solo croce

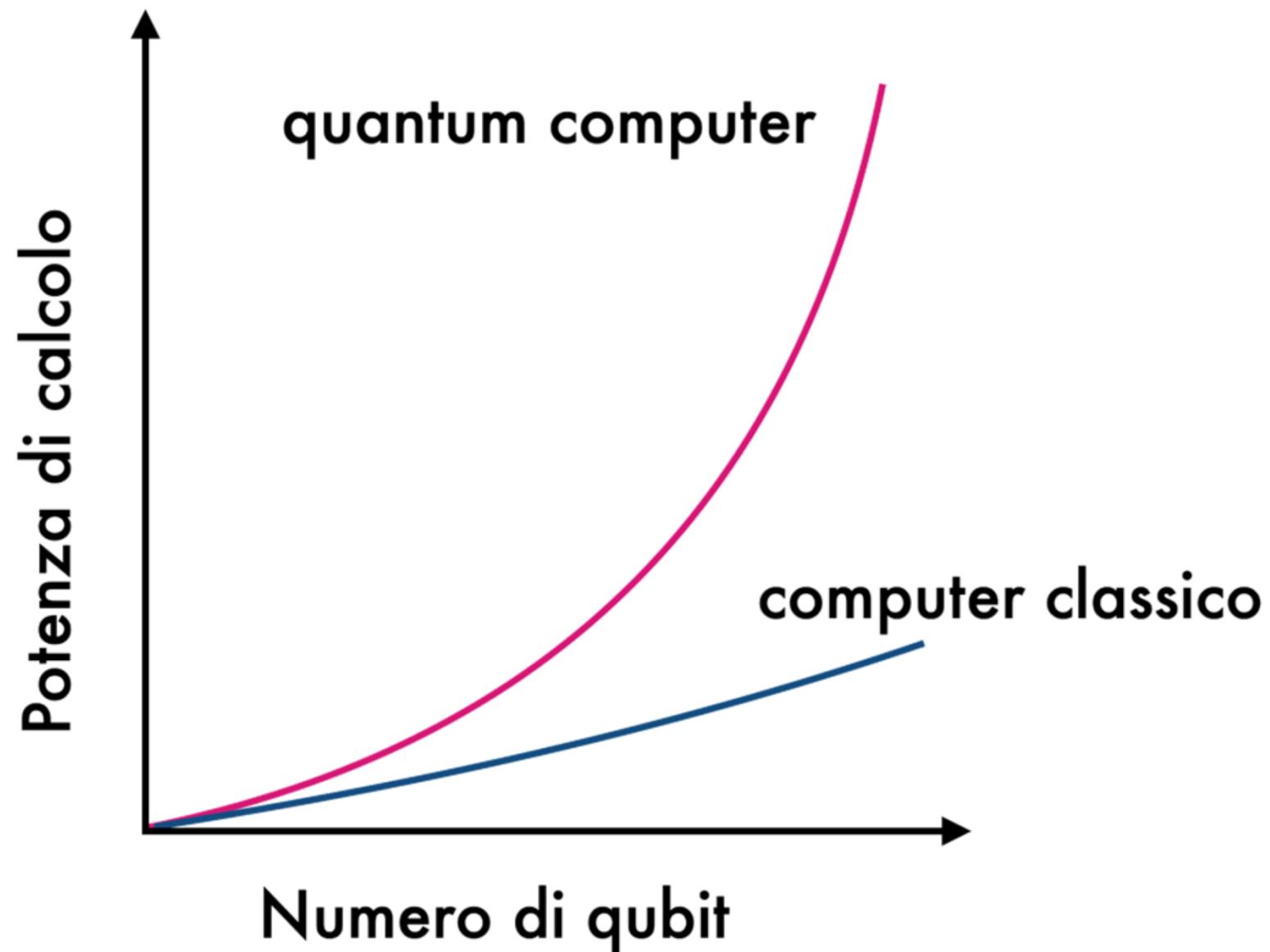


Entanglement: collegamenti “a distanza”

- Due o più qubit possono essere entangled, cioè correlati in modo quantistico
- Lo stato di un qubit è legato allo stato dell'altro, anche se sono lontani
- Se misuriamo uno, l'informazione che otteniamo è collegata immediatamente all'altro



Perché sovrapposizione ed entanglement sono potenti



- Permettono a un sistema quantistico di rappresentare molte configurazioni contemporaneamente
- È come esplorare molte soluzioni di un problema in parallelo invece che una alla volta
- Questo porta a una crescita esponenziale della capacità di calcolo con l'aumentare dei qubit

Esempio: ottimizzazione del traffico in città

- Immaginiamo di voler coordinare tutti i semafori di Torino per ridurre il traffico
- Ogni semaforo può avere diversi stati e orari: il numero di combinazioni esplode
- Un computer quantistico può aiutare a cercare in modo efficiente tra moltissime possibilità



Esempio: il problema del commesso viaggiatore

- Un venditore deve visitare molte città riducendo al minimo il percorso totale
- Aumentando il numero di città, il numero di percorsi possibili cresce in modo esponenziale
- È un problema classico di ottimizzazione, difficile per i computer tradizionali



Altri problemi complessi nel mondo reale



- Gestione di risorse in ospedali, industrie o reti di trasporto
- Scelta ottimale di investimenti finanziari con molti vincoli
- Simulazione accurata di sistemi fisici e chimici con tante particelle

Ambiti applicativi del quantum computing



- Finanza: analisi del rischio e ottimizzazione di portafogli
- Telecomunicazioni: gestione ottimale delle reti e delle frequenze
- Sanità: pianificazione di visite, terapie, logistica di farmaci e dispositivi

Altre applicazioni potenziali

- Chimica e materiali: simulazione di molecole e nuovi materiali
- Sicurezza informatica: nuovi schemi di crittografia e generazione di numeri casuali
- Intelligenza artificiale: nuovi algoritmi di machine learning quantistico



Quantum computing e computer classici

- I computer quantistici non sostituiscono quelli tradizionali
- Sono strumenti complementari, adatti a problemi specifici e molto complessi
- In futuro useremo sistemi ibridi: parte classica e parte quantistica che lavorano insieme

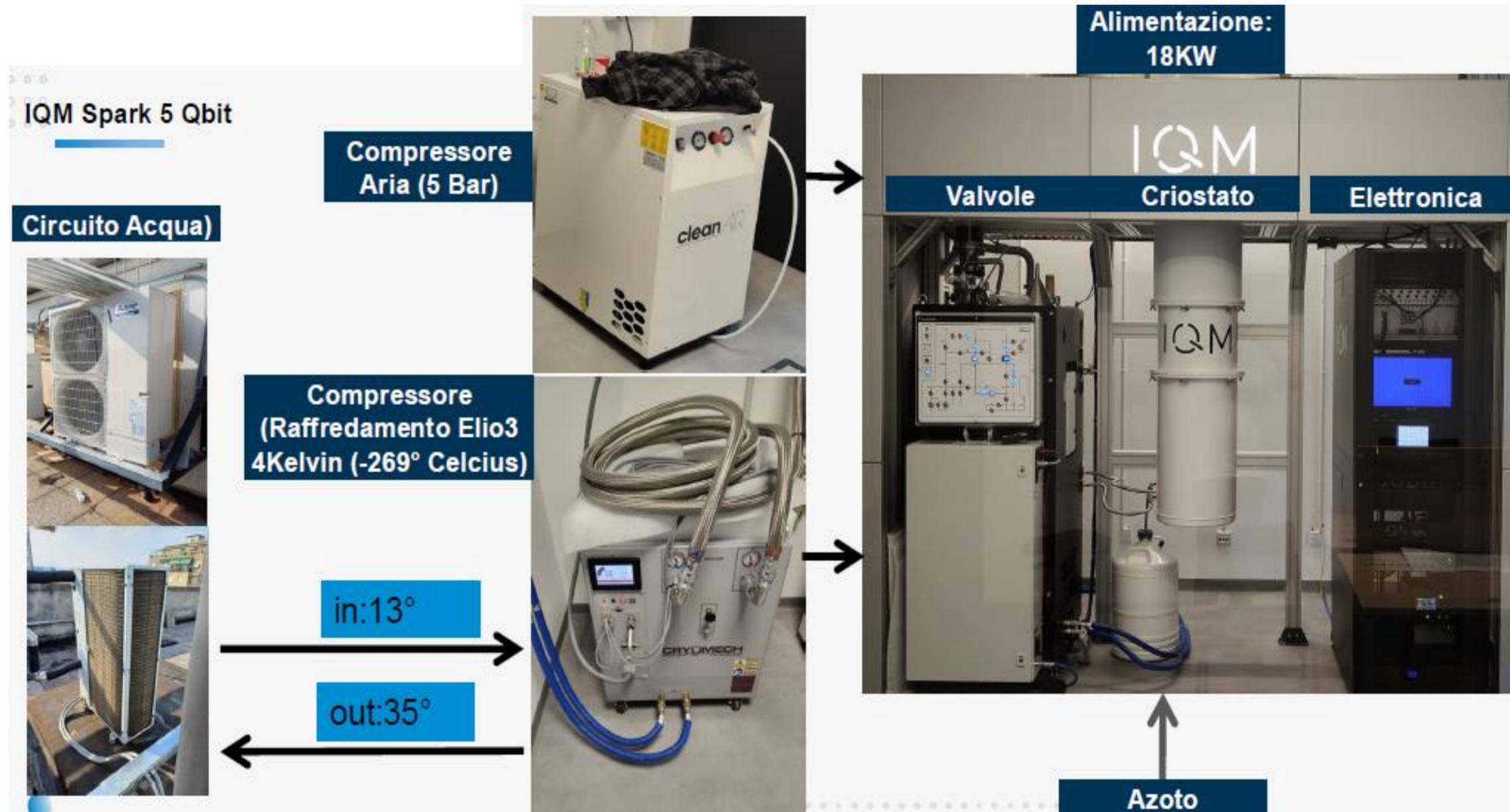


Il contesto al Politecnico di Torino

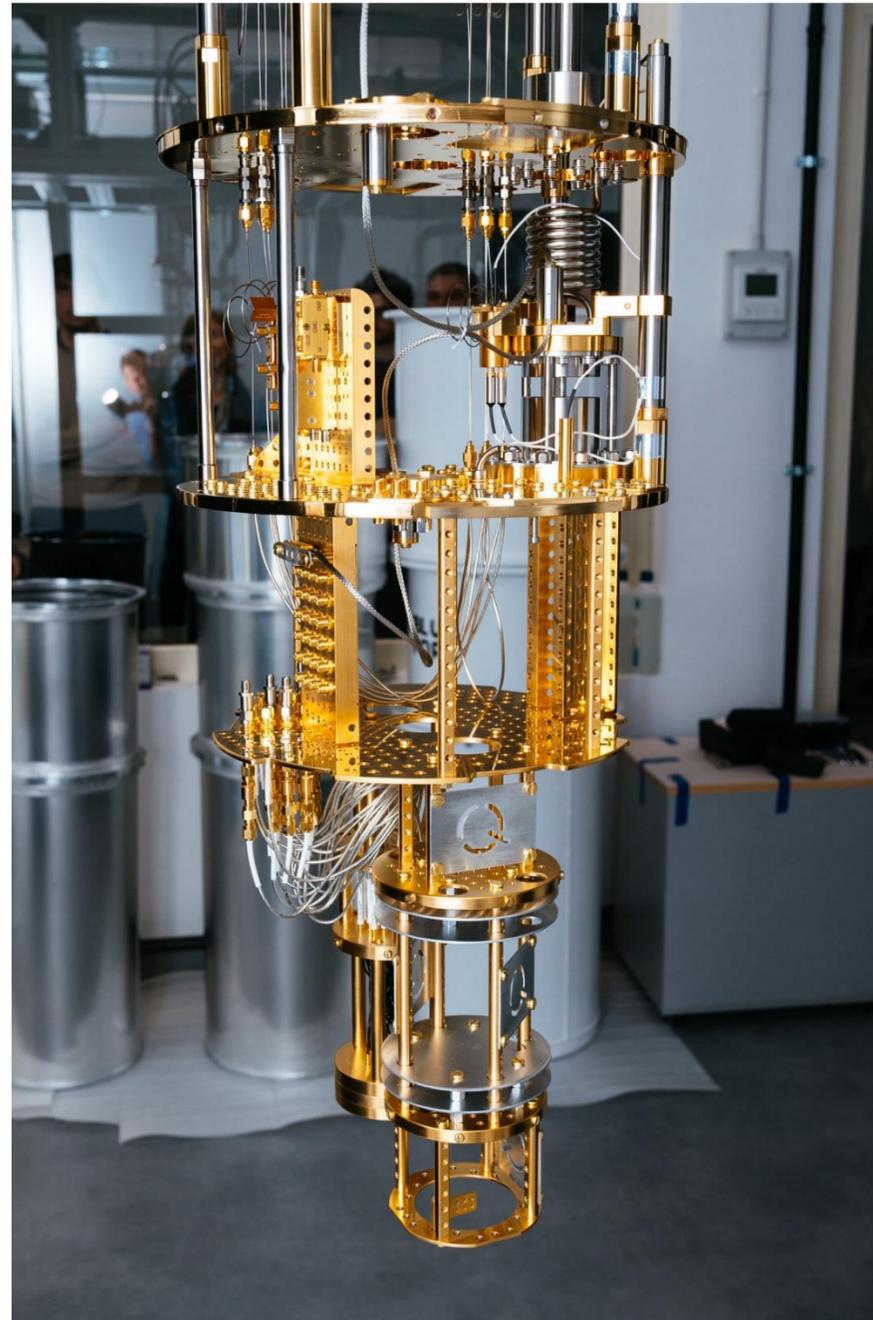
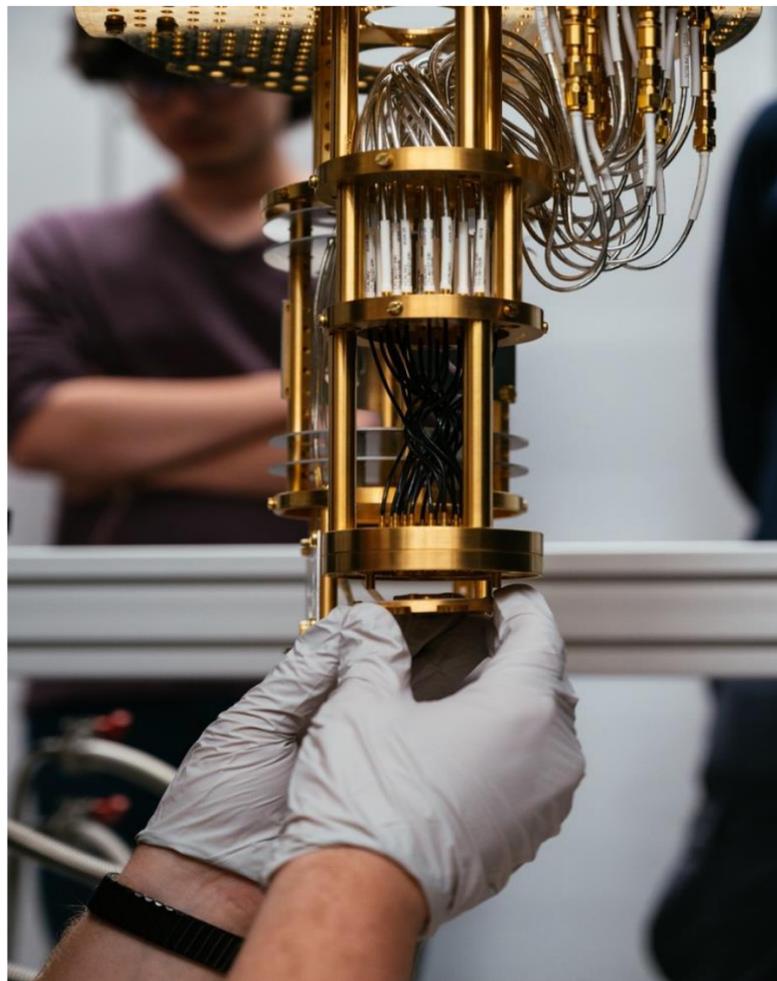


- Il Politecnico di Torino ha installato un computer quantistico reale
- La macchina è fornita dall'azienda europea IQM ed stata *battezzata* "Lagrange"
- È il primo computer quantistico di questo tipo in Italia utilizzato in ambito universitario

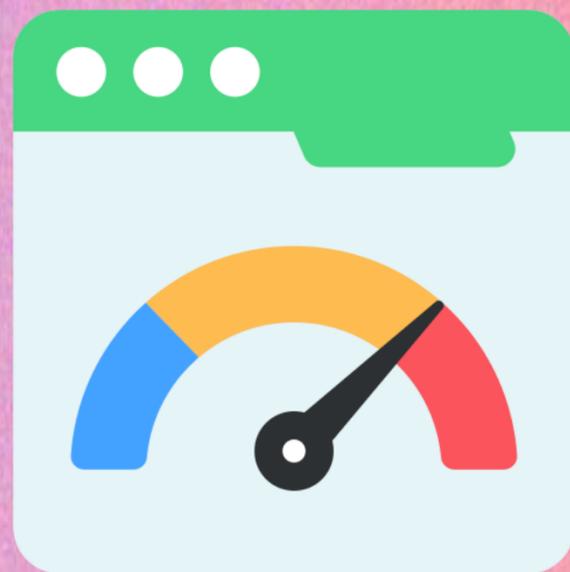
IQM "Lagrange"



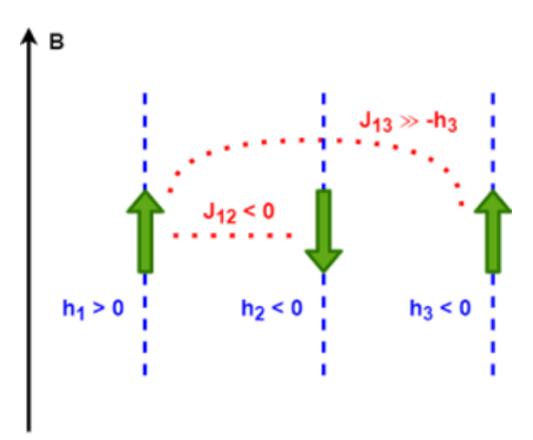
IQM "Lagrange"



Quantum Optimizations

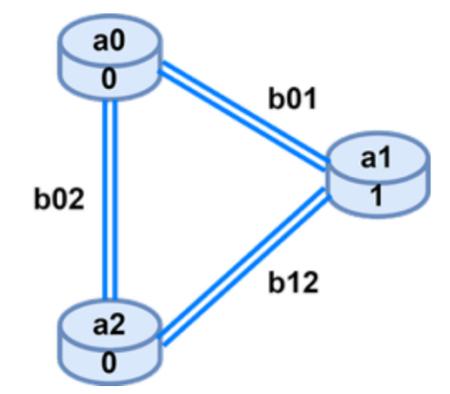


Solving optimization problems

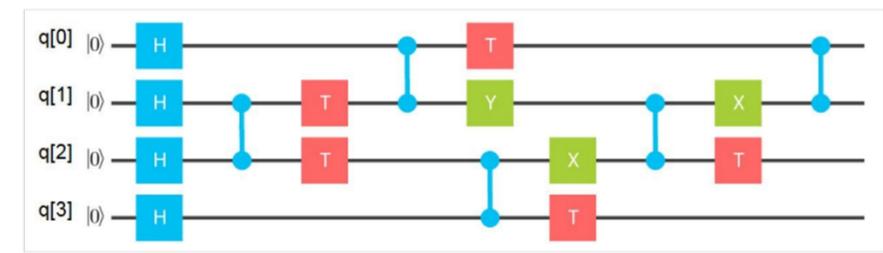
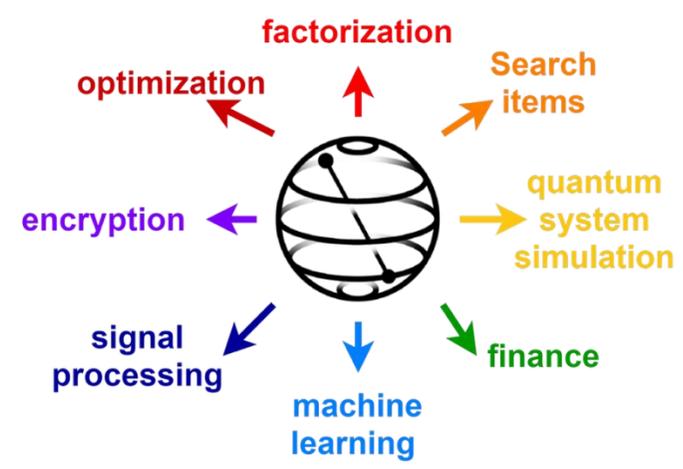


ISING FORMULATION
(Bipolar variables)
[Ising formulation](#)

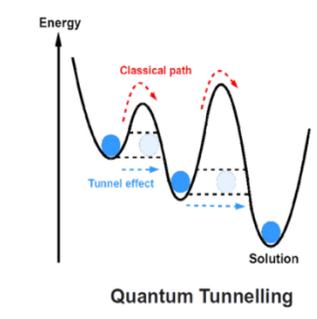
QUBO FORMULATION
(Unipolar variables)
[Qubo formulation tutorial](#)



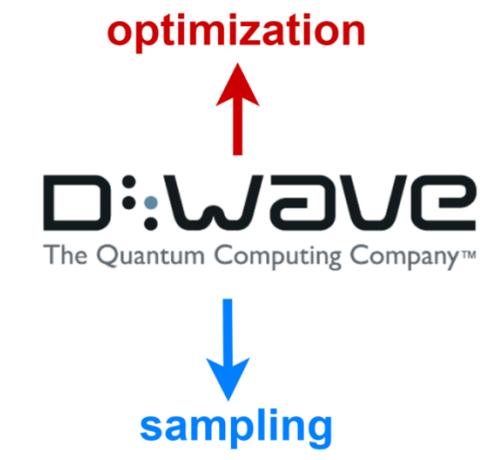
Quantum Paradigm



Quantum Gate Array



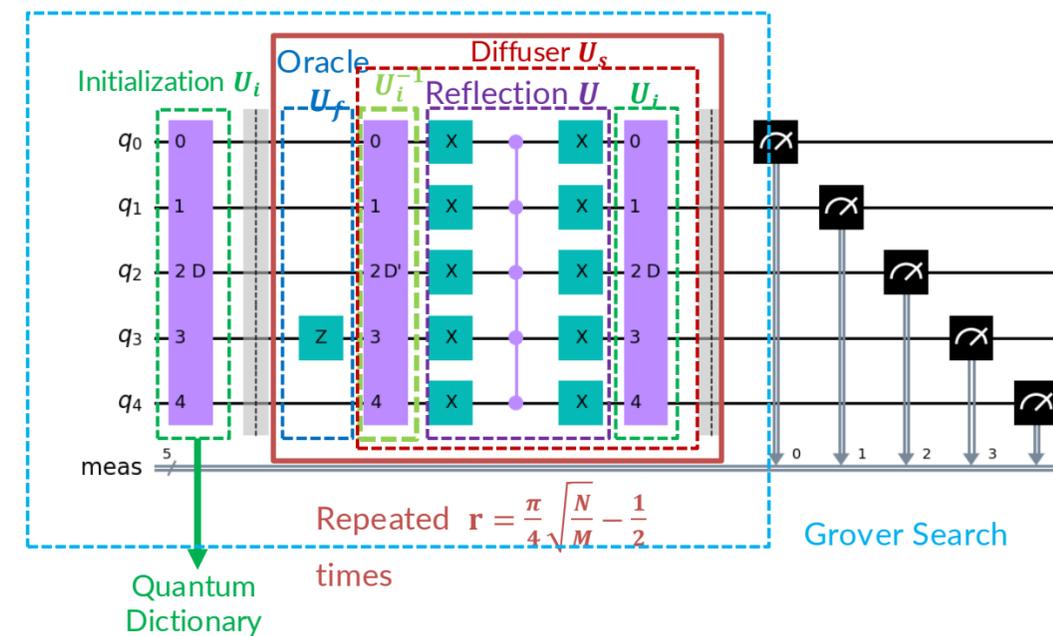
Quantum Annealing



Solving optimization problems

Our thesis proposals in this context spans from:

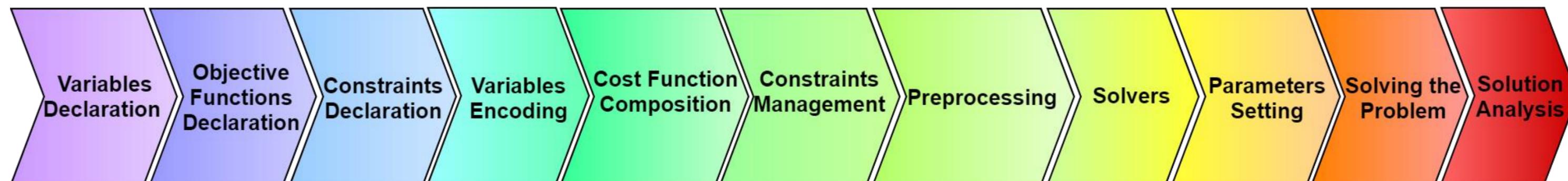
- Solver development/improvement



Solving optimization problems

Our thesis proposals in this context spans from:

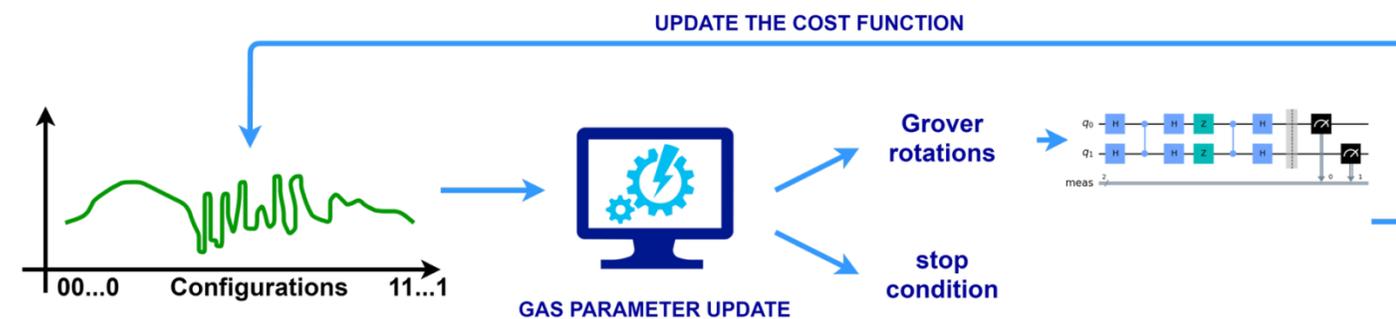
- Solver development/improvement



Solving optimization problems

Our thesis proposals in this context spans from:

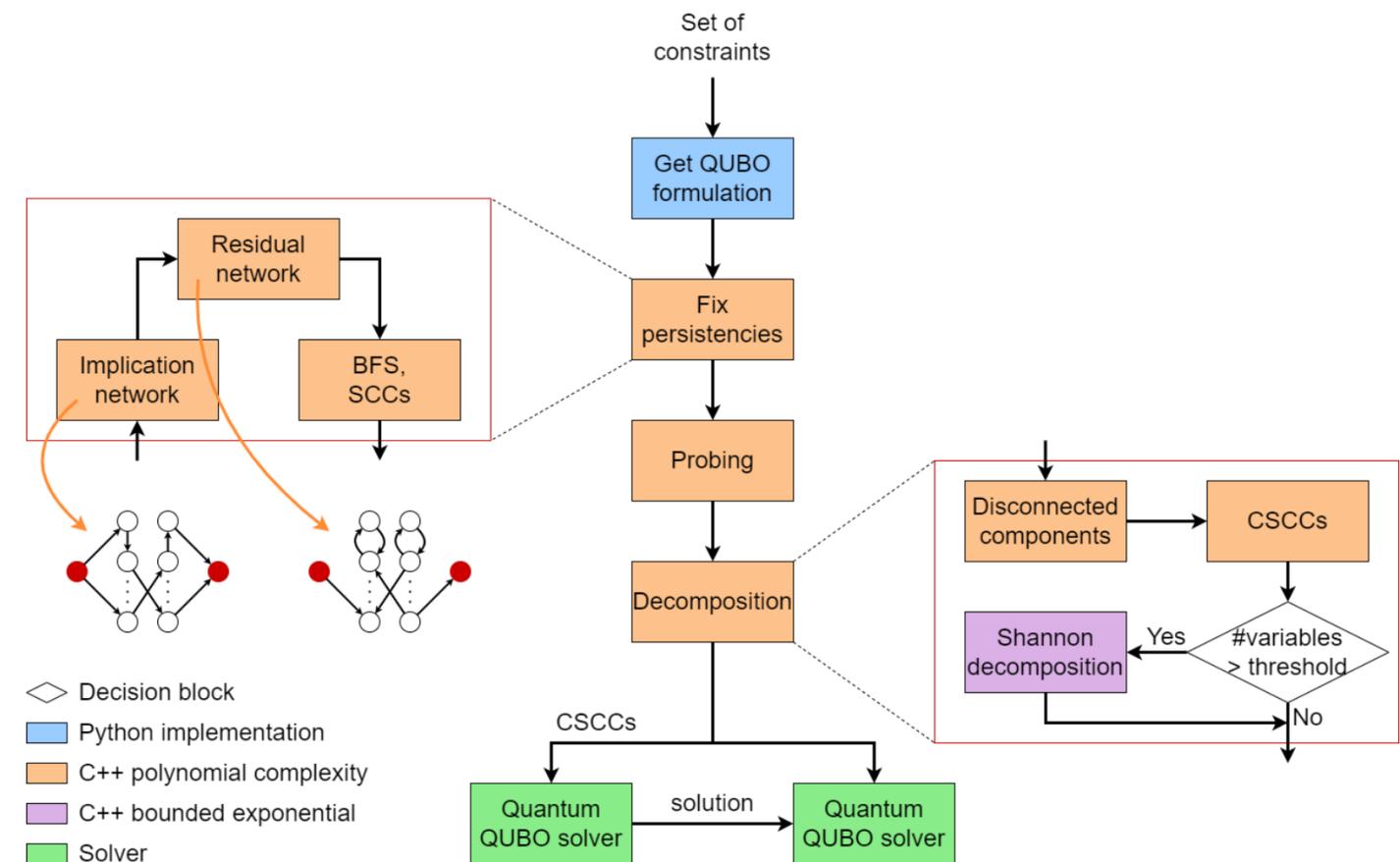
- Solver development/improvement
- Automating QUBO formulation
- Detecting optimal solver settings



Solving optimization problems

Our thesis proposals in this context spans from:

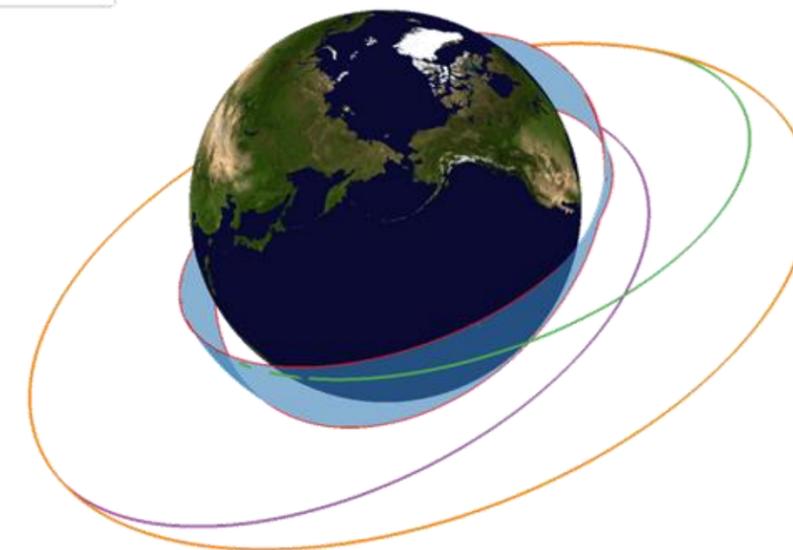
- Solver development/improvement
- Automating QUBO formulation
- Detecting optimal solver settings
- QUBO Reduction
- Development of QUBO formulation for specific optimization problems



Solving optimization problems

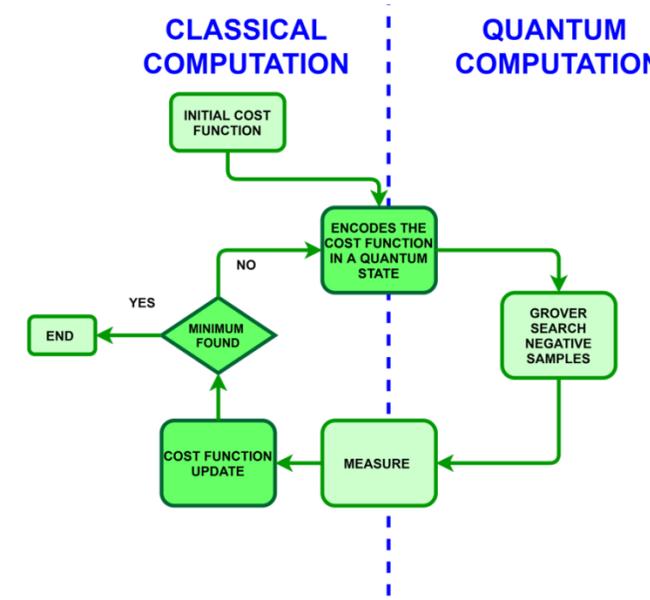
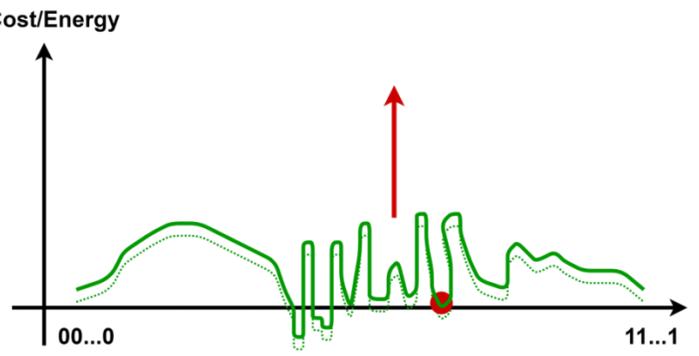
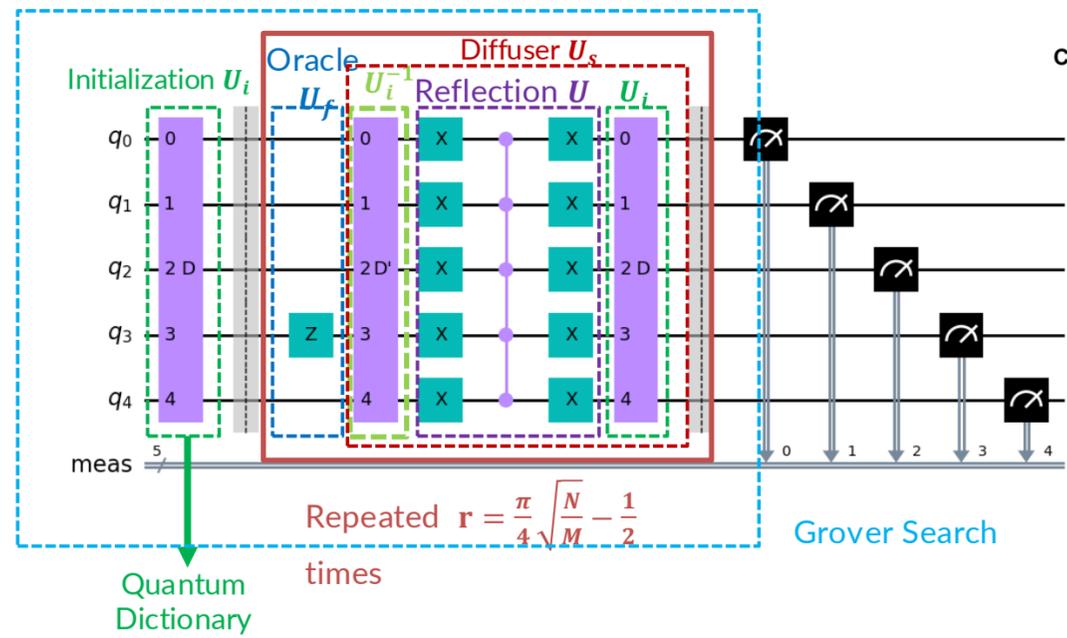
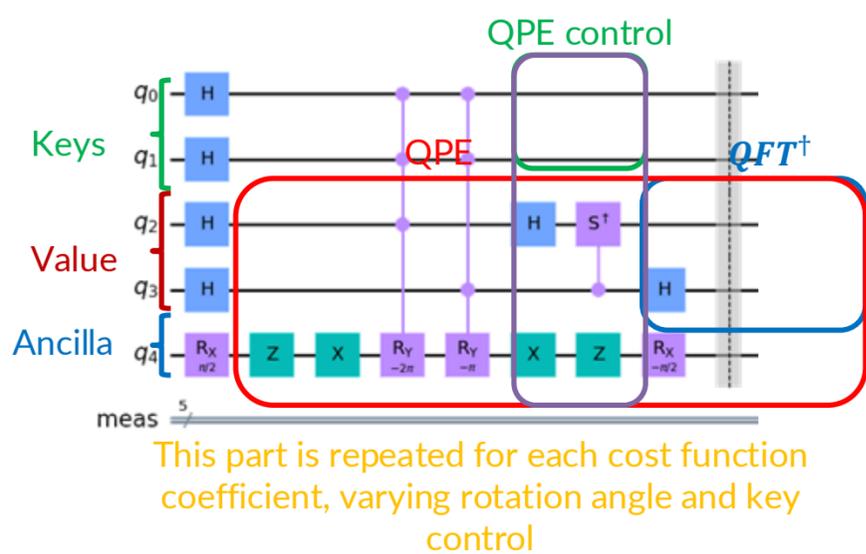
Our thesis proposals in this context spans from:

- Solver development/improvement
- Automating QUBO formulation
- Detecting optimal solver settings
- QUBO Reduction
- Development of QUBO formulation for specific optimization problems



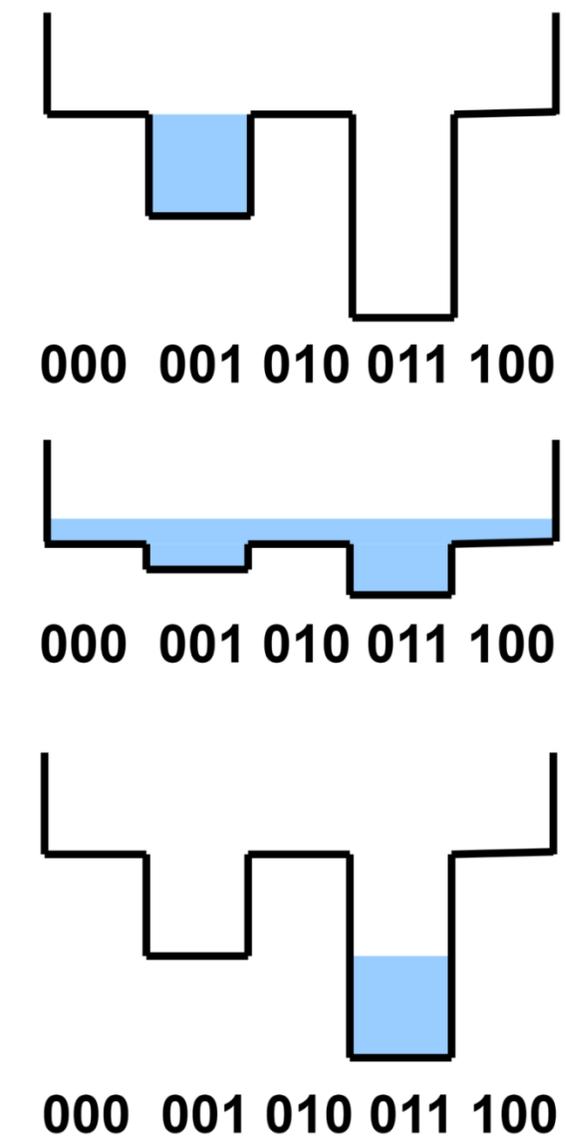
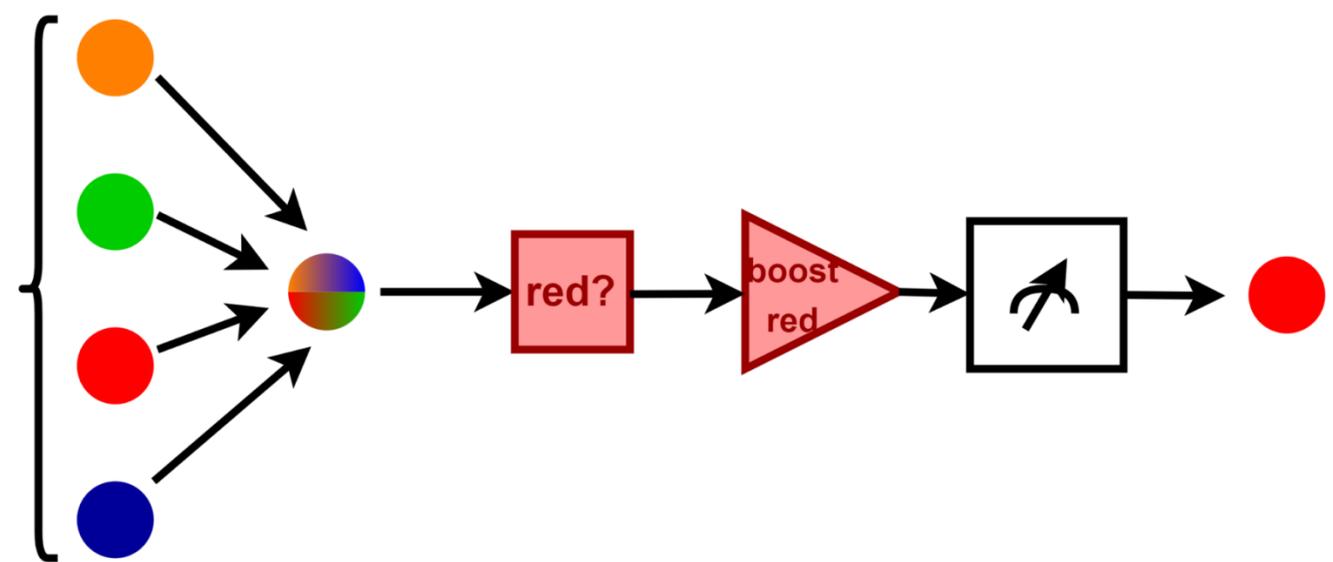
Grover Adaptive Search

- Cost Function preconditioning implementation to reduce as much as possible the number of qubits required for value
- Implementation of an automatic approach for setting the initial threshold



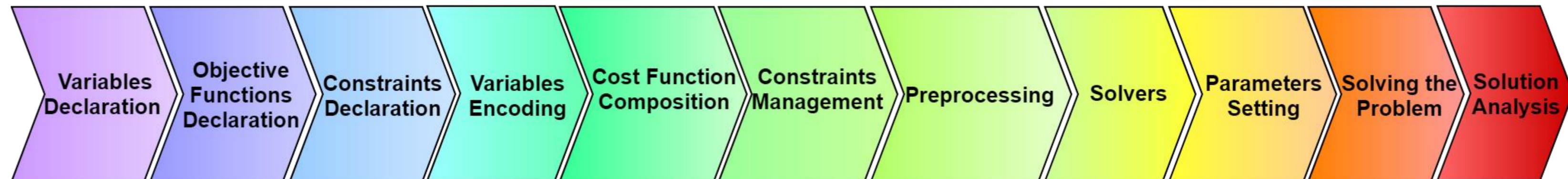
Quantum-Assisted Genetic Algorithm

- Study and implementation of classical genetic algorithm
- Study of the quantum assisted genetic algorithm
- Implementation in qiskit-compatible format
- Study of the degrees of freedom
- Comparison of quantum and classical counterpart



Polynomial Reduction and constraint generation

- Study of methods for polynomial reduction (from PUBO/HUBO to QUBO)
- Cython module for implementing various method
- Performance evaluation
- Study of penalty functions generation from constraint (with particular focus on inequality and reducing the number of auxiliary) and implementation in Cython



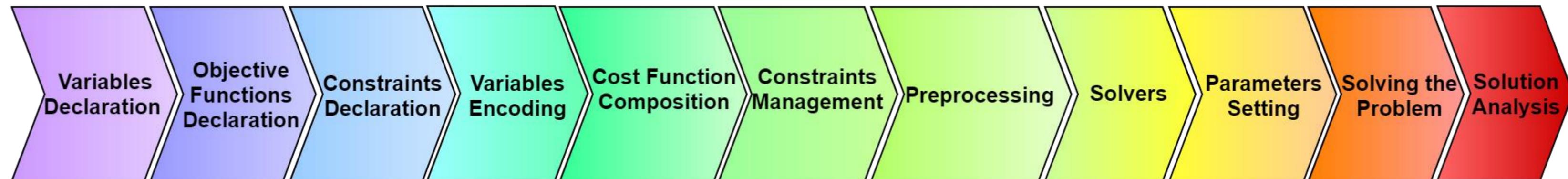
Montanez-Barrera, J.; Willsch, D.; Maldonado-Romo, A.; Michielsen, K. [Unbalanced penalization: A new approach to encode 1895inequality constraints of combinatorial problems for quantum optimization algorithms.](#) Quantum Science and Technology 2024, 18969, 025022..

Schmidbauer, Lukas, et al. "[Polynomial Reduction Methods and their Impact on QAOA Circuits.](#)" arXiv preprint arXiv:2406.08889 (2024).
D. Volpe, N. Quetschlich, M. Graziano, G. Turvani, and R. Wille, "[Towards an automatic framework for solving optimization problems with quantum computers,](#)" IEEE International Conference on Quantum Software (QSW), 2024.



Approximation of non-polynomial functions and variable encoding

- Study of methods for polynomialization of a generic function
- Cython implementation of the step
- Performance evaluation, identifying the validity bound of the approximation
- Study and implementation of variable encoding mechanism in Cython



Pauckert, Justin, et al. "[Autoqubo v2: Towards efficient and effective qubo formulations for ising machines.](#)" Proceedings of the Companion Conference on Genetic and Evolutionary Computation. 2023.

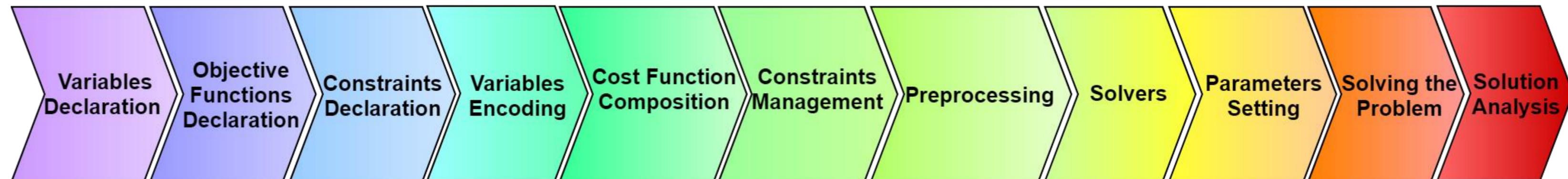
Novara, Carlo, Mattia Boggio, and Deborah Volpe. "[Quantum optimization for Nonlinear Model Predictive Control.](#)" arXiv preprint arXiv:2410.19467 (2024)

D. Volpe, N. Quetschlich, M. Graziano, G. Turvani, and R. Wille, "[Towards an automatic framework for solving optimization problems with quantum computers,](#)" IEEE International Conference on Quantum Software (QSW), 2024.



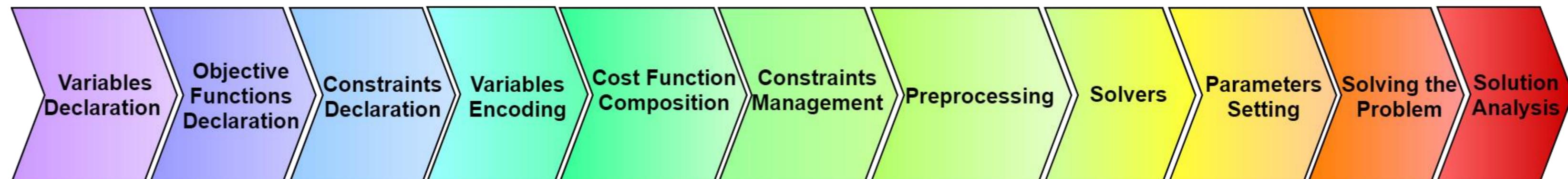
Best Solver settings

- Develop a machine-learning model that, given a QUBO instance, predicts the optimal configuration parameters for a chosen quantum gate-array quantum solver.
- Needed to label the dataset, define the best ML model, evaluate the performance.



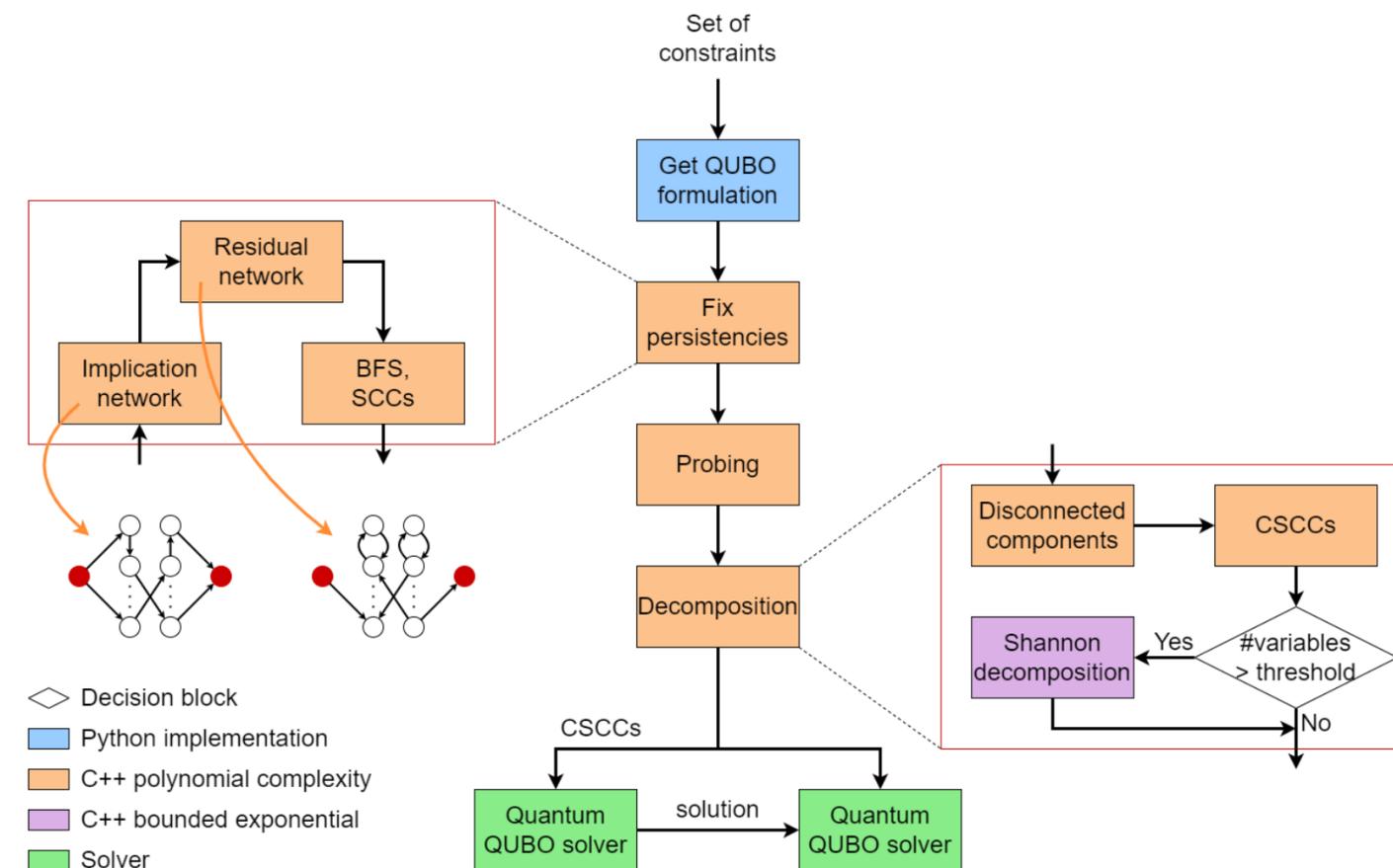
Best Lambda

- Develop a machine-learning model that, given a QUBO instance, predicts the optimal λ
- Needed to label the dataset, define the best ML model, evaluate the performance.

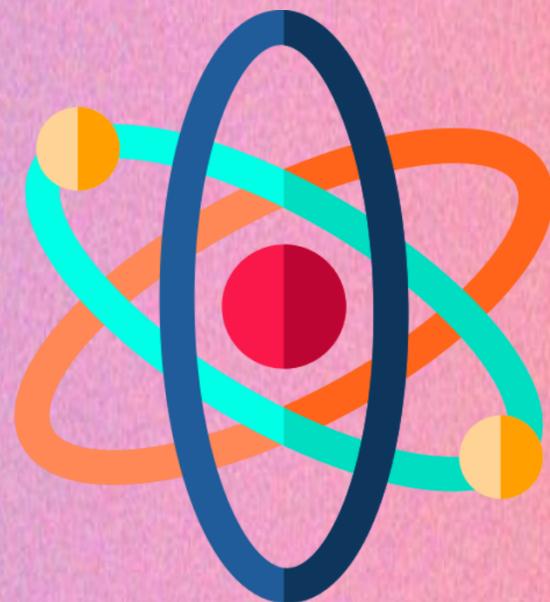


Decomposition and Reduction

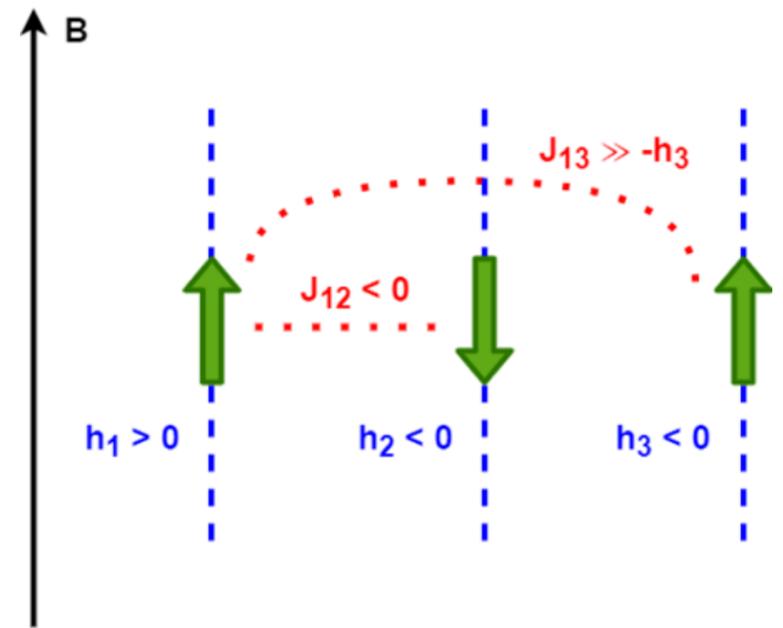
- Expansion of the Decomposition methods supported by the Qoolchain
- Implementation of quadratic persistencies identification
- Implementation of QUBO sparsification methods for reducing the connectivity degree
- Implementation of Embedding algorithm
- Possible recognition of complexity P or NP given an input problem



Ising Machines

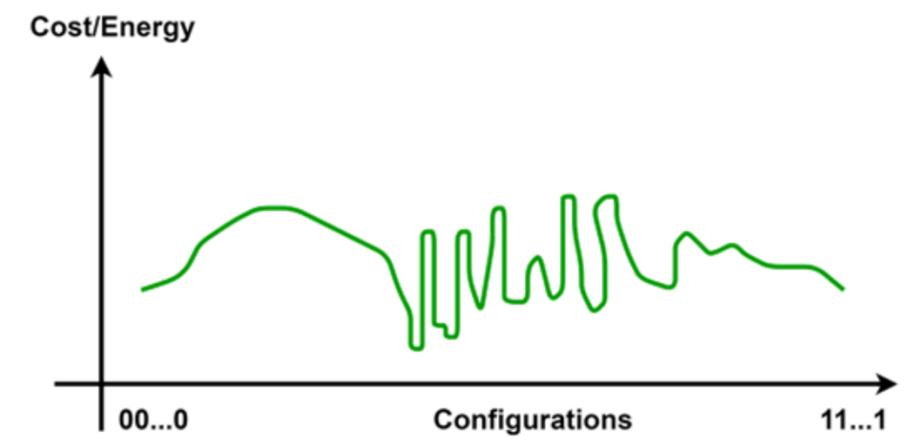


Hardware Design of Ising Machines

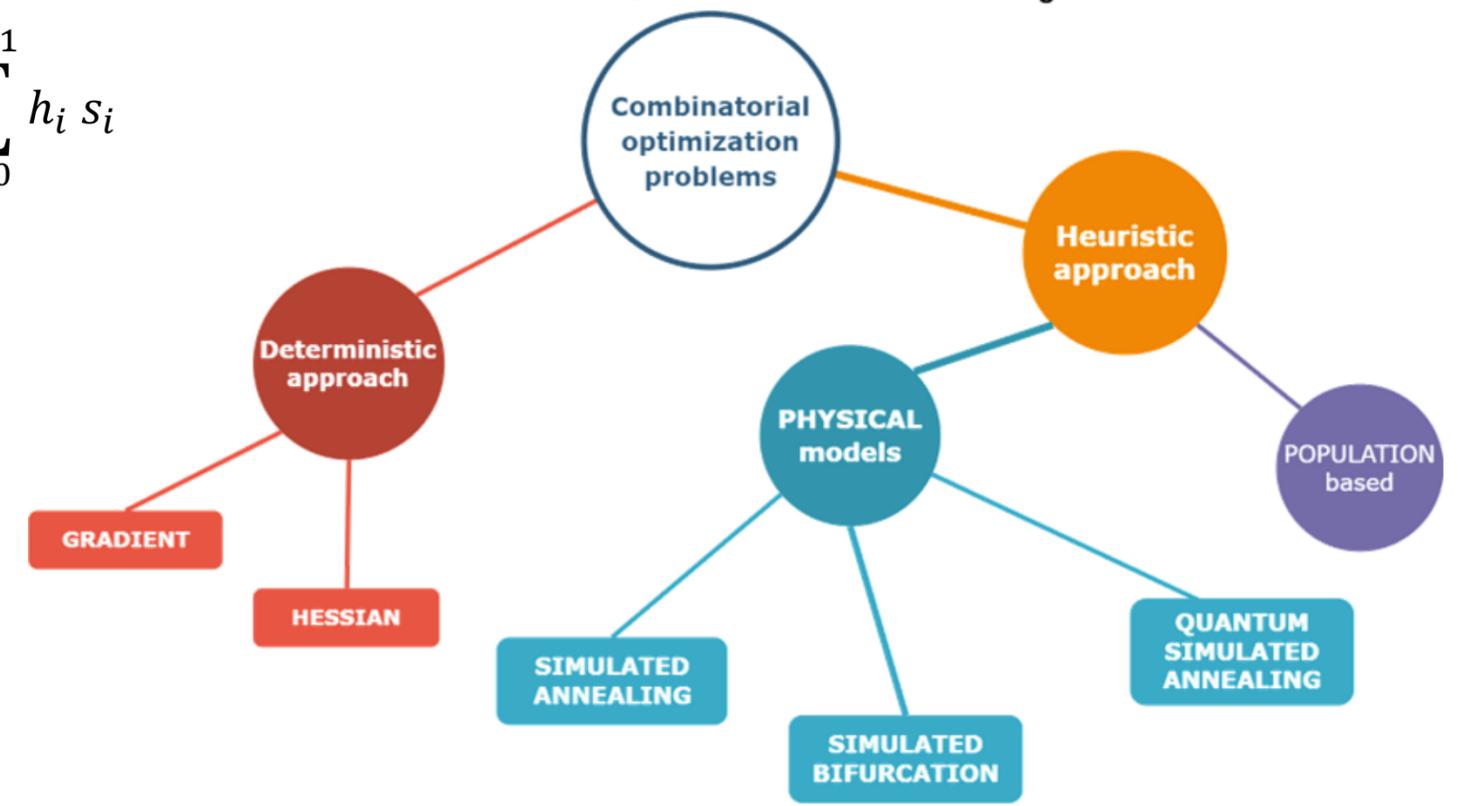


Ising Model: a physical mathematical problem of ferromagnetism, usually employed for describing combinatorial optimization problems.

$$H = \frac{1}{2} \sum_{i=0}^{N-1} \sum_{j=0, j \neq i}^{N-1} J_{ij} S_i S_j + \sum_{i=0}^{N-1} h_i S_i$$



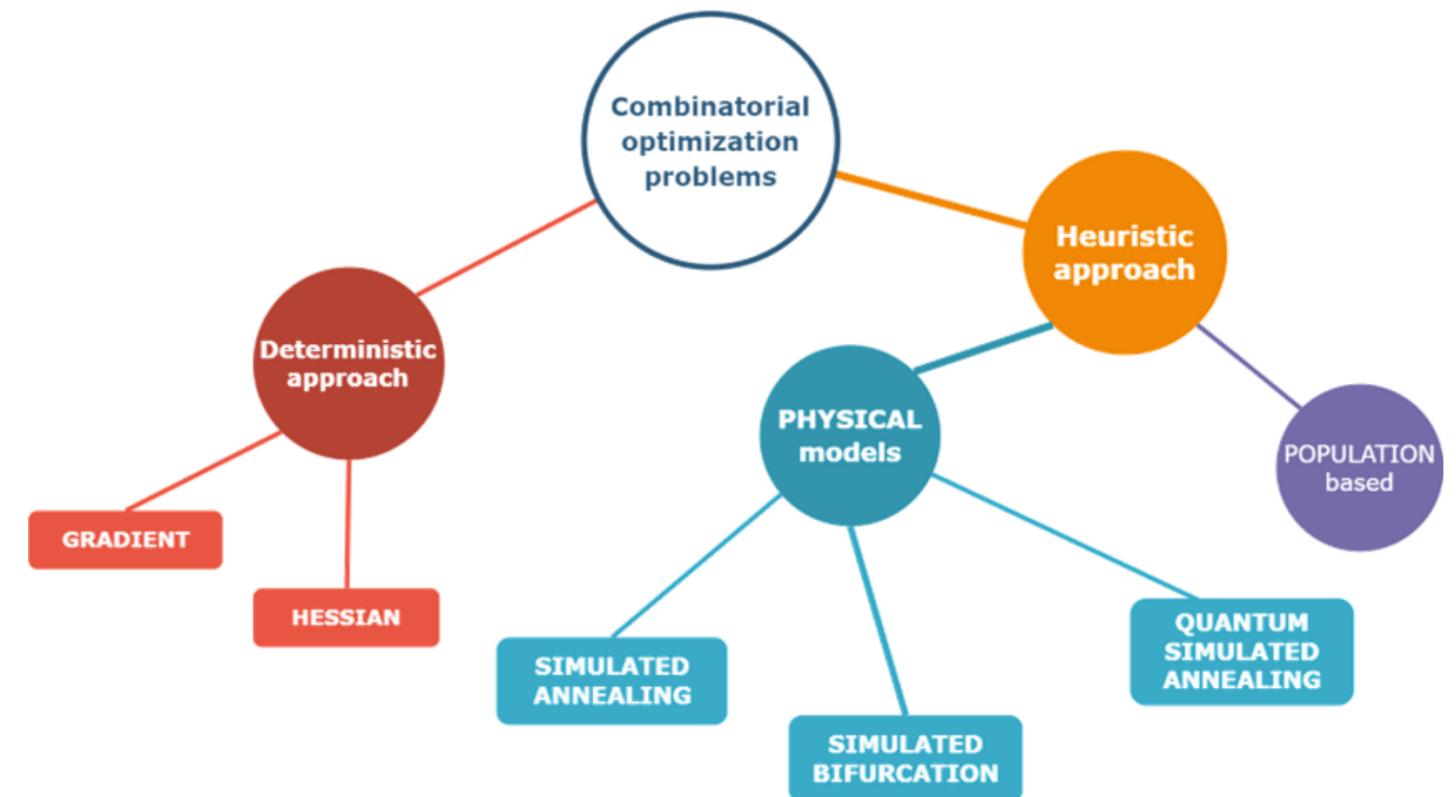
Ising Machines: any hardware specifically designed for finding the ground state of the Ising model.



Hardware Design of Ising Machines

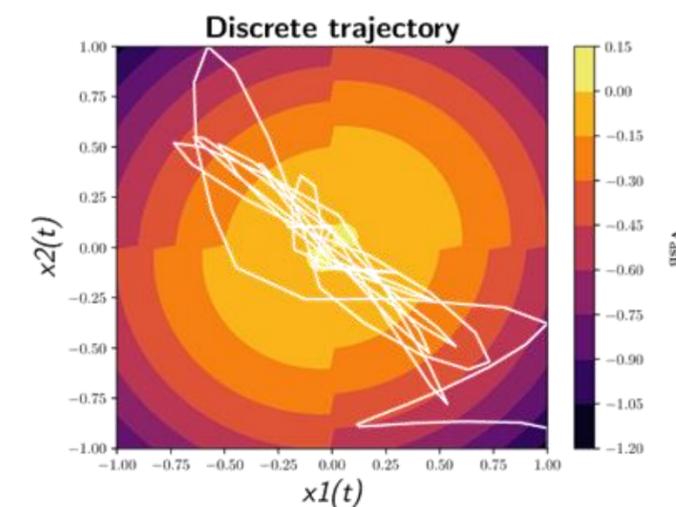
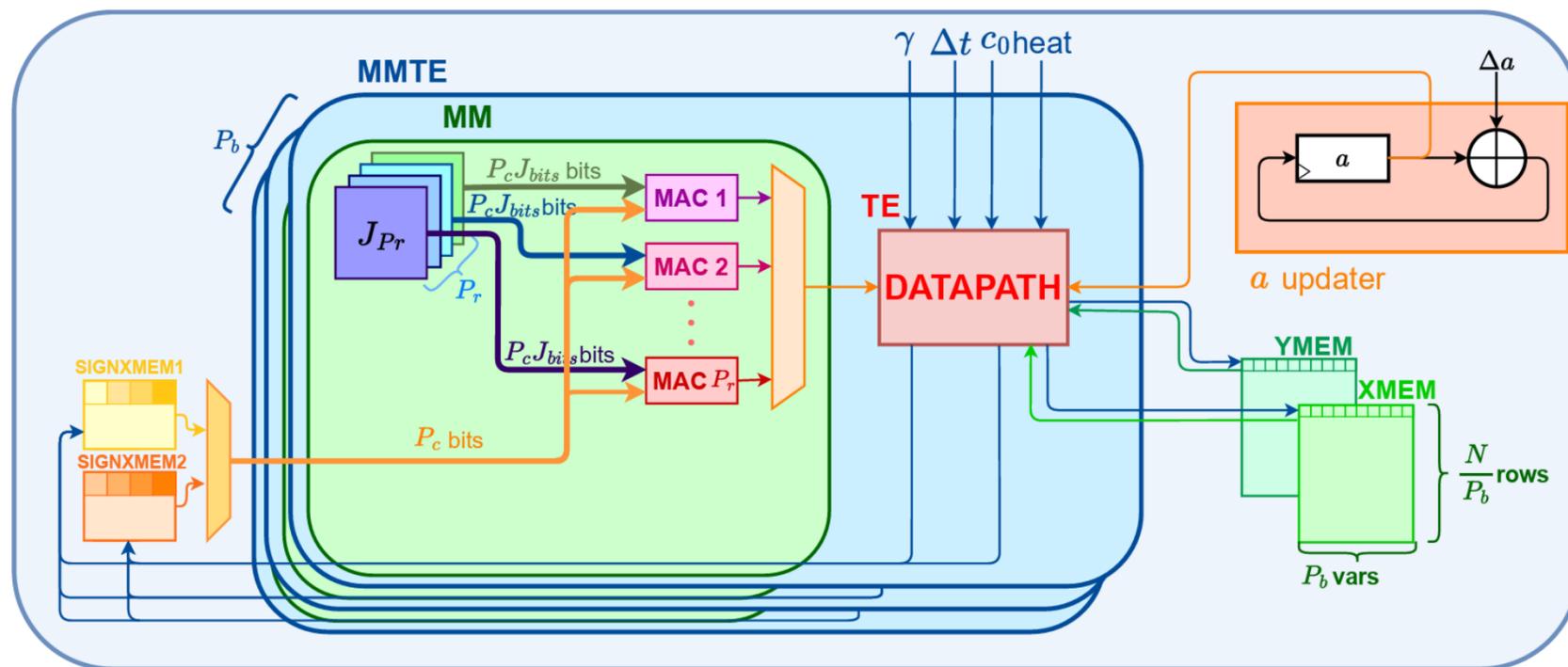
Our thesis proposals in this context requires:

- Algorithmic analysis
- Software modelling
- Hardware design (HDL or HLS)
- On-board validation



SBRINZ, Higher Order SBM

Improving an existing dSB architecture supporting higher-order problems, starting from the software model and HDL description

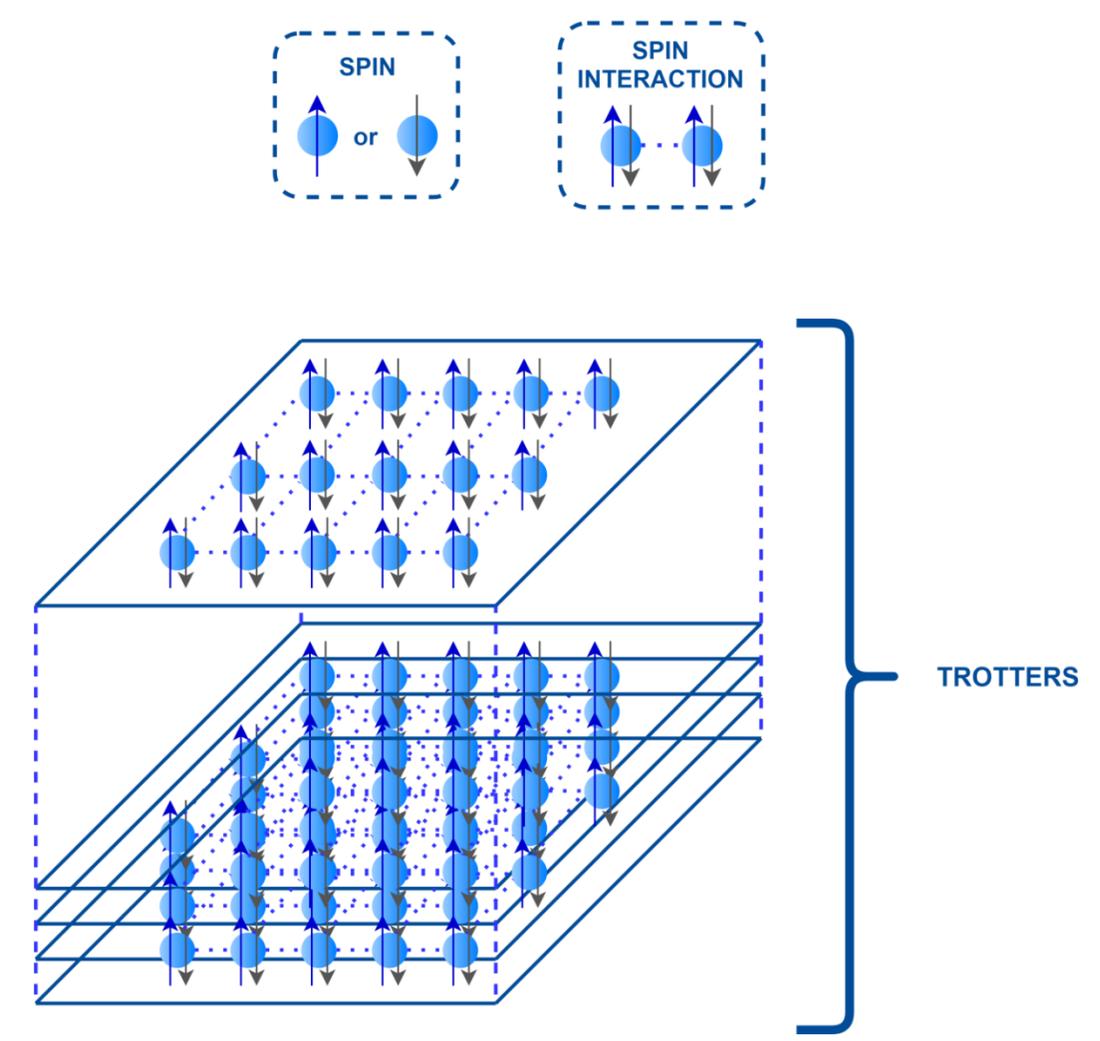


Kanao, Taro, and Hayato Goto. "[Simulated bifurcation for higher-order cost functions.](#)" Applied Physics Express 16.1 (2022): 014501.



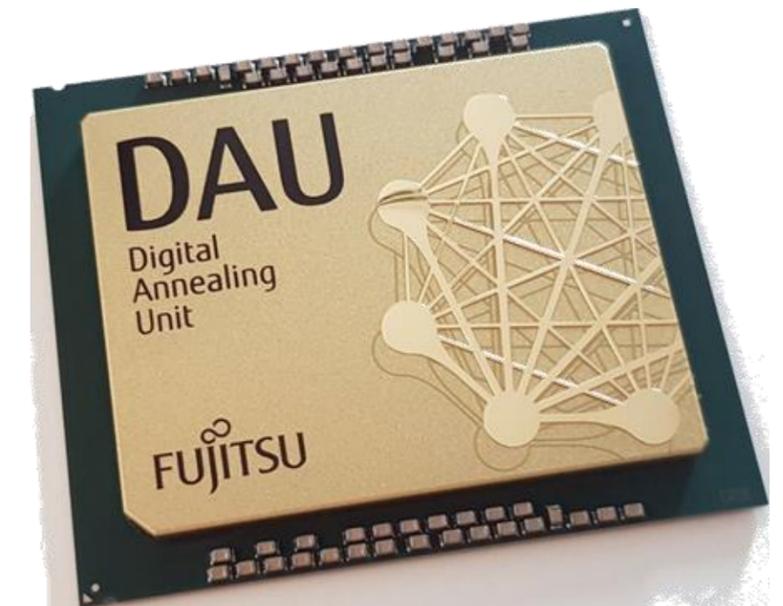
T.IM.2: Simulated Quantum Annealing

- SQA algorithm is a probabilistic method which permits to solve combinatorial optimization problems on digital computers, exploiting the operating principles of a quantum computer
- Development of Cython software implementation starting from the python one
- Design of the hardware implementation



Digital Annealer

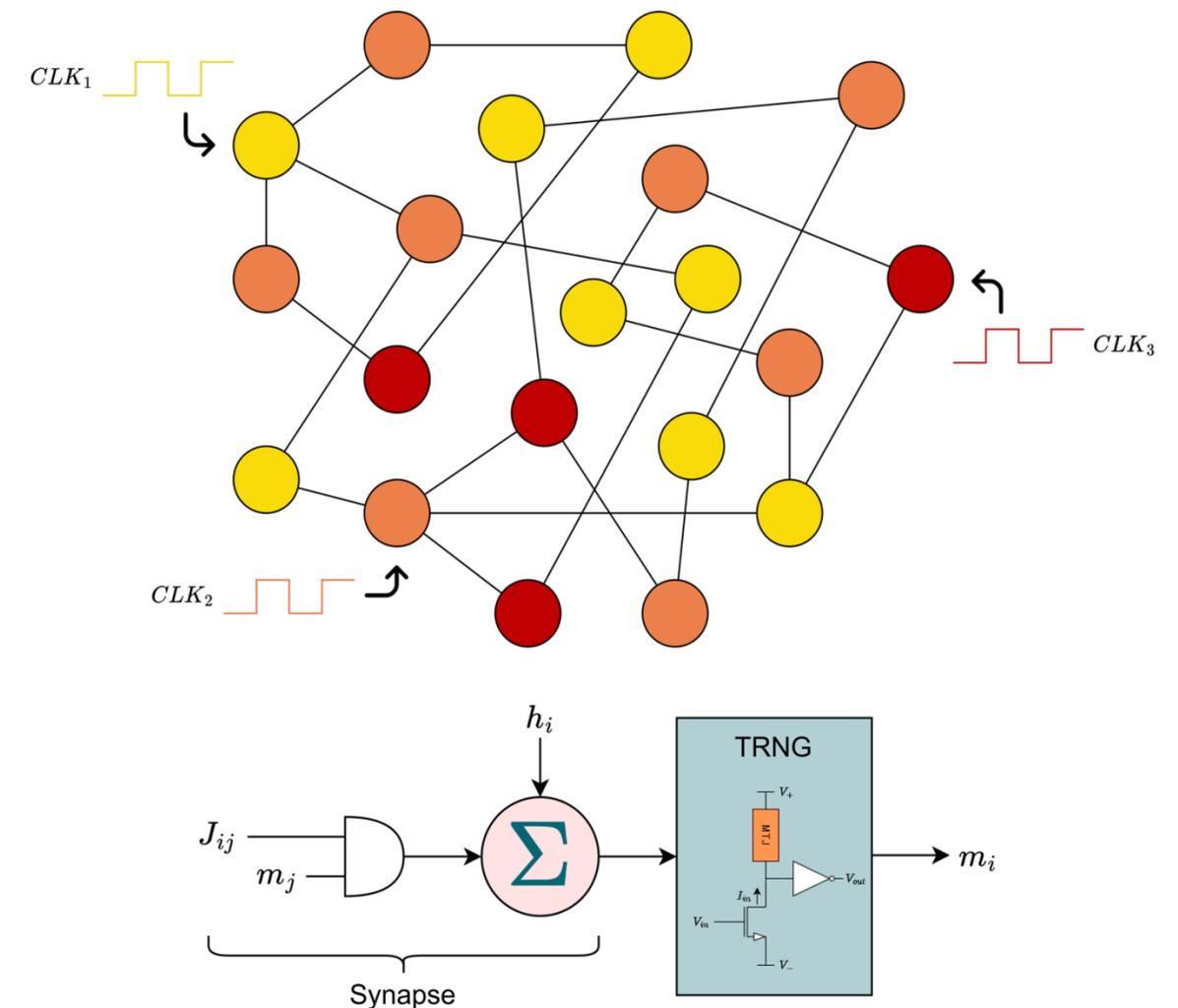
- The DA is a quantum-inspired computing solution to solve large scale combinatorial optimization problems. It gives better results than simulated annealing approach for fully-connected problems
- Evaluation of benefit of integrating a Tabu search-like mechanism
- Development of Cython software implementation starting from the python one
- Design of the hardware implementation



Probabilistic Computing Emulation

Object: Development of an FPGA-based emulator of a probabilistic computer.

- Analysis of the most suitable optimization procedure and native graph for problem embedding.
- RTL design and synthesis of a probabilistic computer with a pseudo random number generator.
- Evaluation of the optimal implementation features according to the problem characteristics.



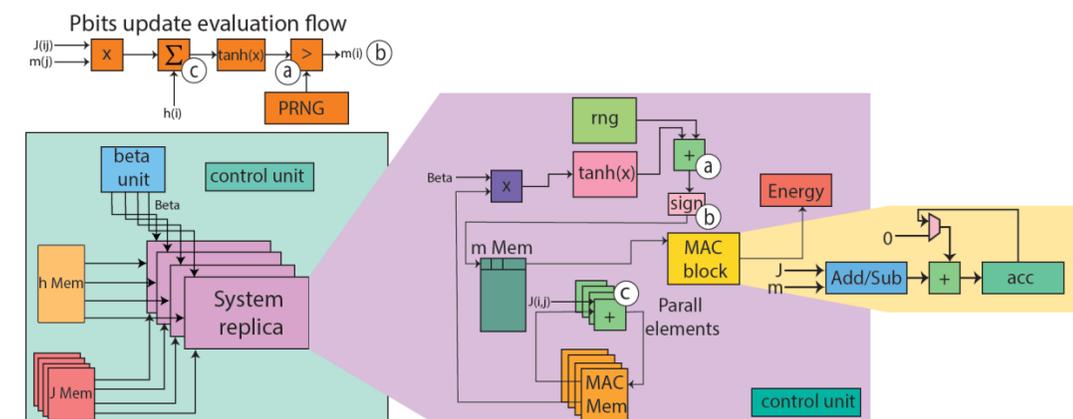
Probabilistic Ising Machine

The thesis aims at improving an existing fully digital Probabilistic Ising Machine (PIM) architecture implemented on FPGA. The proposed activities will focus on architectural and micro-architectural optimizations to improve scalability, performance, and resource efficiency. In particular, the improvements may include:

- **Design and implementation of a caching mechanism to efficiently exploit both off-chip DDR memory and on-chip BRAM, reducing memory bandwidth bottlenecks.**
- **Development of hyperbolic tangent evaluation units without relying on LUT-based implementations.**

The work will involve architectural design, RTL implementation, and experimental validation on FPGA platforms.

*In collaboration with the prof. Giovanni Finocchio of University of Messina



Requirements:

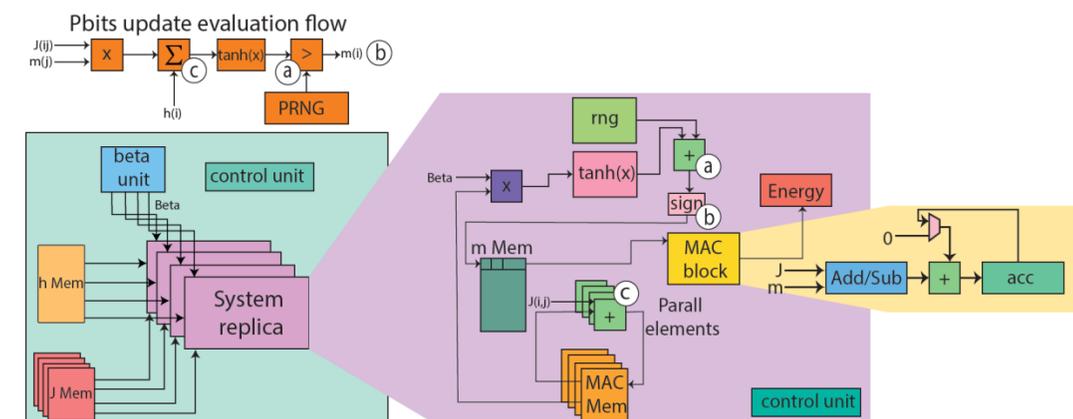
- Experience with SystemVerilog for RTL design
- Familiarity with Xilinx Vivado tools for synthesis and implementation

Probabilistic Ising Machine

The thesis aims at **designing and integrating an annealing-schedule evolution unit (β -unit)** within an existing Probabilistic Ising Machine (PIM) architecture, enabling the implementation of advanced optimization algorithms such as **Parallel Tempering** and **Simulated Quantum Annealing**.

The work will involve **architectural design, RTL implementation, and experimental validation on FPGA platforms**.

*In collaboration with the prof. Giovanni Finocchio of University of Messina



Requirements:

- Experience with SystemVerilog for RTL design
- Familiarity with Xilinx Vivado tools for synthesis and implementation

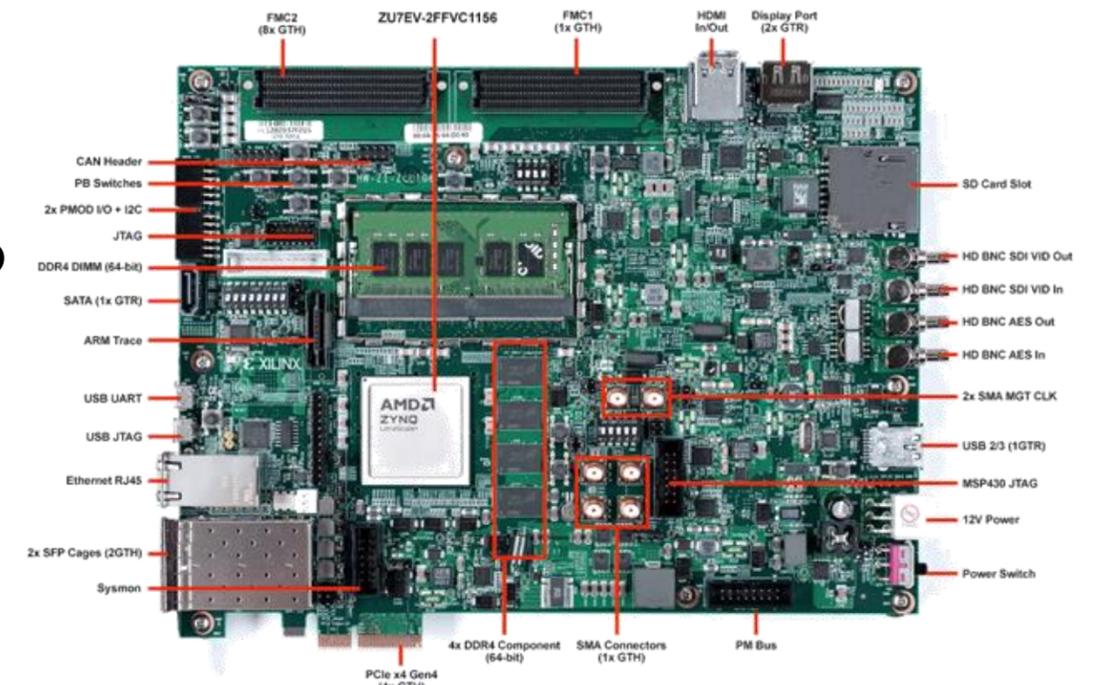
PCIExpress

The objective of this thesis is to design and implement a **PCI Express (PCIe) communication interface** for FPGA-based accelerators deployed on the **AMD Zynq UltraScale+ ZCU106 platform**.

The goal is to enable **high-throughput, low-latency communication** between a host system and custom hardware accelerators implemented in the programmable logic.

The developed PCIe interface will be integrated into an existing hardware–software acceleration framework, enabling efficient data transfer and control of FPGA-based computation kernels from the host.

*In collaboration with the prof. Giovanni Finocchio of University of Messina

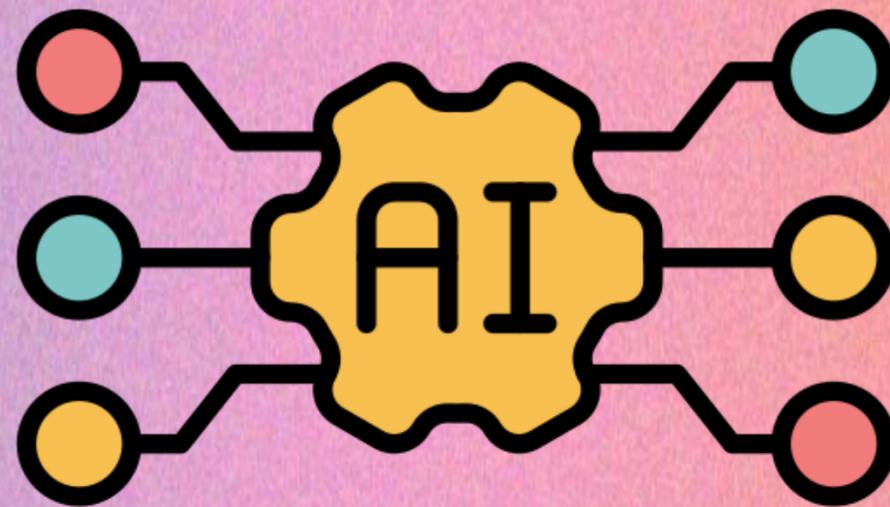


Requirements:

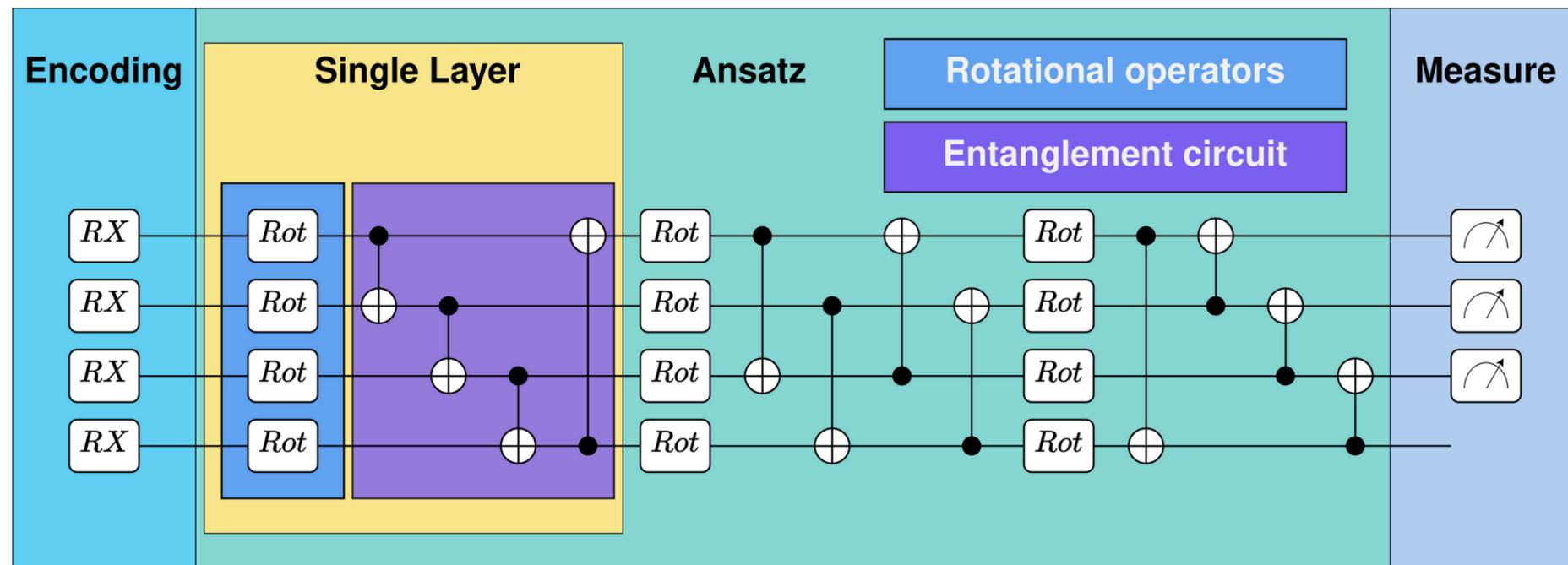
- Experience with SystemVerilog for RTL design
- Familiarity with Xilinx Vivado tools for synthesis and implementation



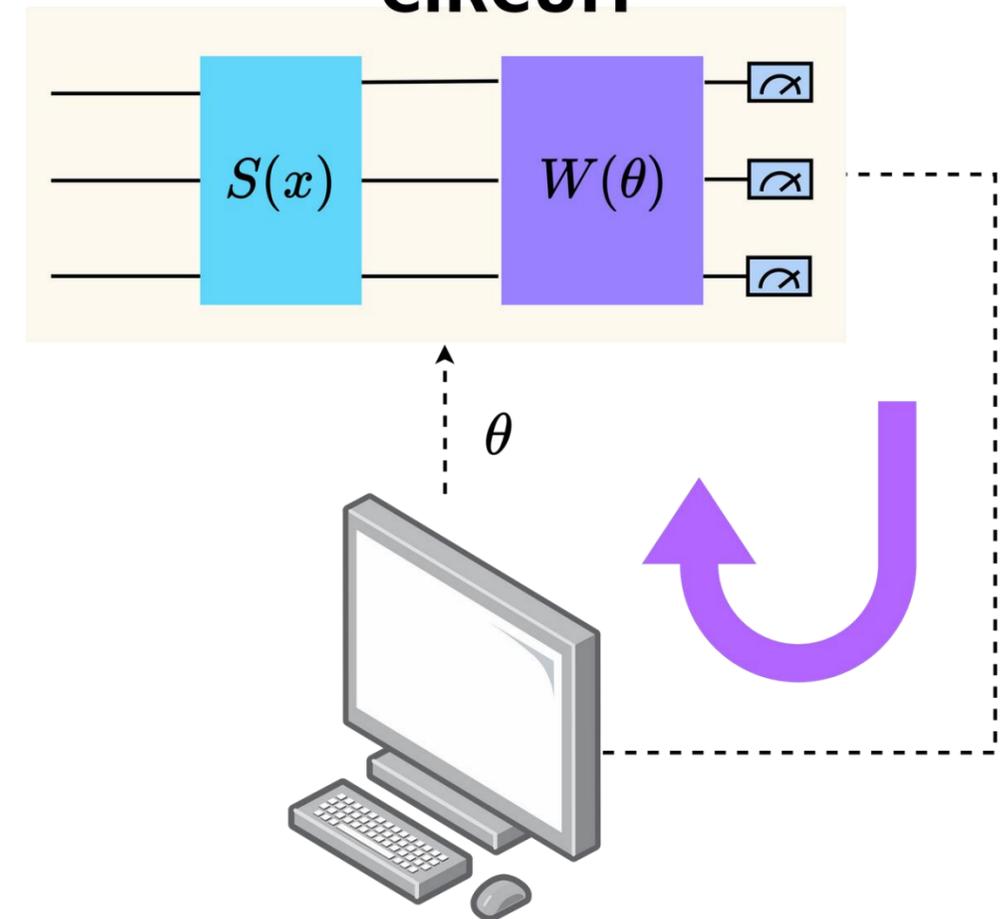
Quantum Machine Learning



Quantum Neural Network



VARIATIONAL QUANTUM CIRCUIT



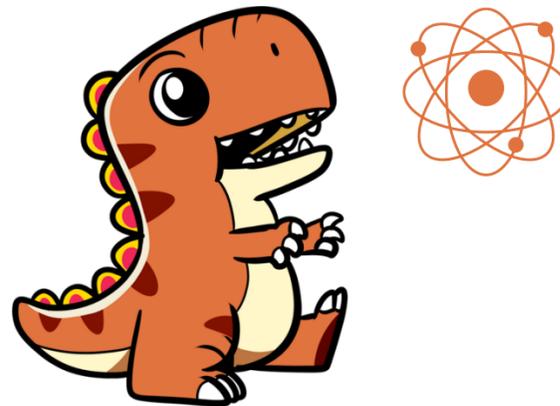
CLASSICAL OPTIMIZER

[Tudisco, A., Volpe, D., Ranieri, G., Curato, G., Ricossa, D., Graziano, M., & Corbelleto, D. \(2024\). Evaluating the computational advantages of the Variational Quantum Circuit model in Financial Fraud Detection. IEEE Access.](#)

QML Models Toolchain

QUAPTOR

QUantum Applications framework Politecnico di TORino



QML

OPTIMIZATION

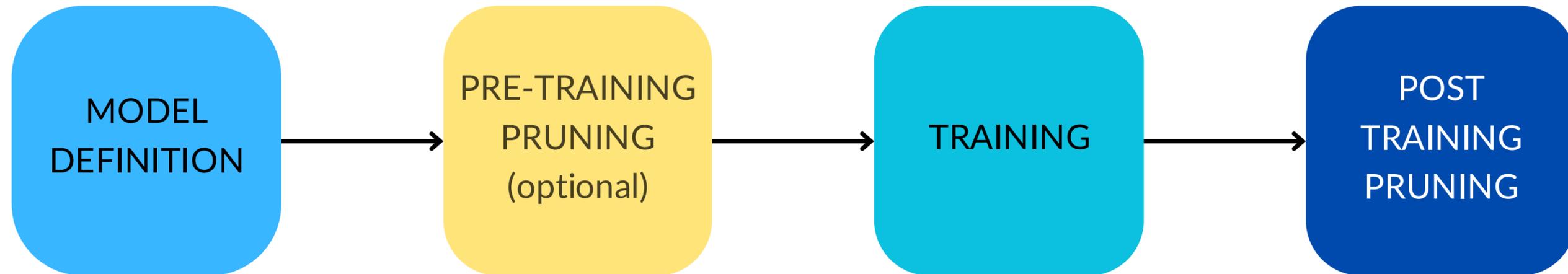
BACK-END



Politecnico
di Torino

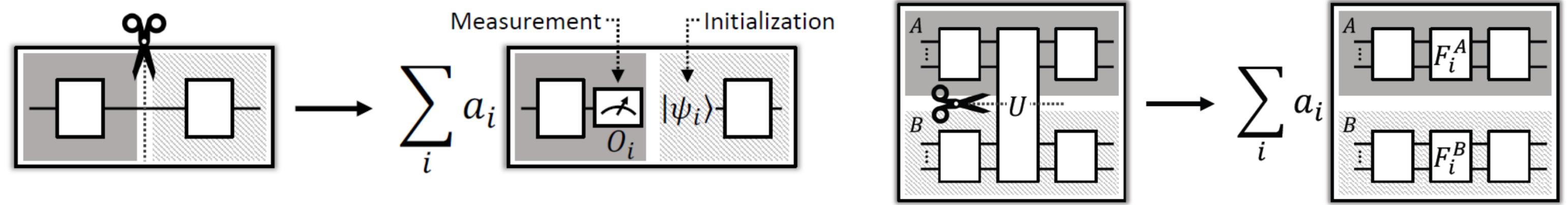
T.QML.1: Pruning technique

Implementation of pruning techniques in QNN models

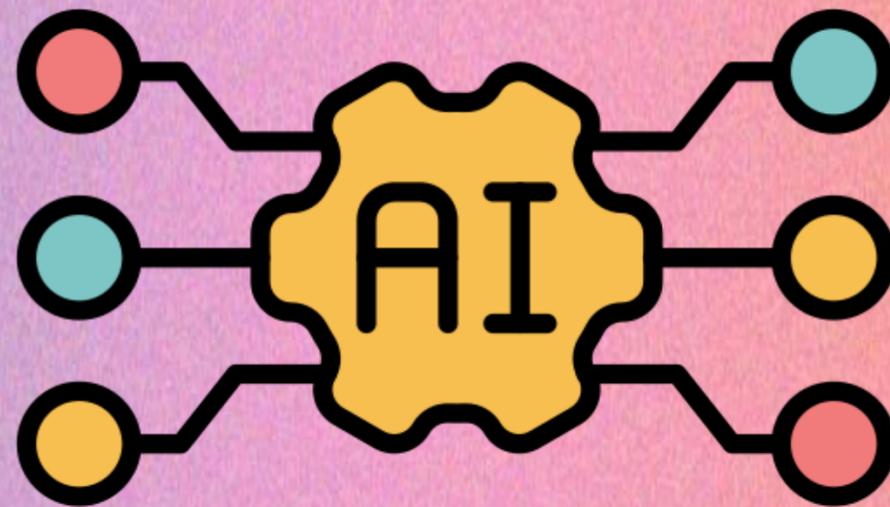


T.QML.2: Circuit decomposition for improving model robustness

Evaluation of the noise impact in each layer and in each portion of QNN model, evaluating the insertion of error mitigation techniques between layers to prevent error propagation.

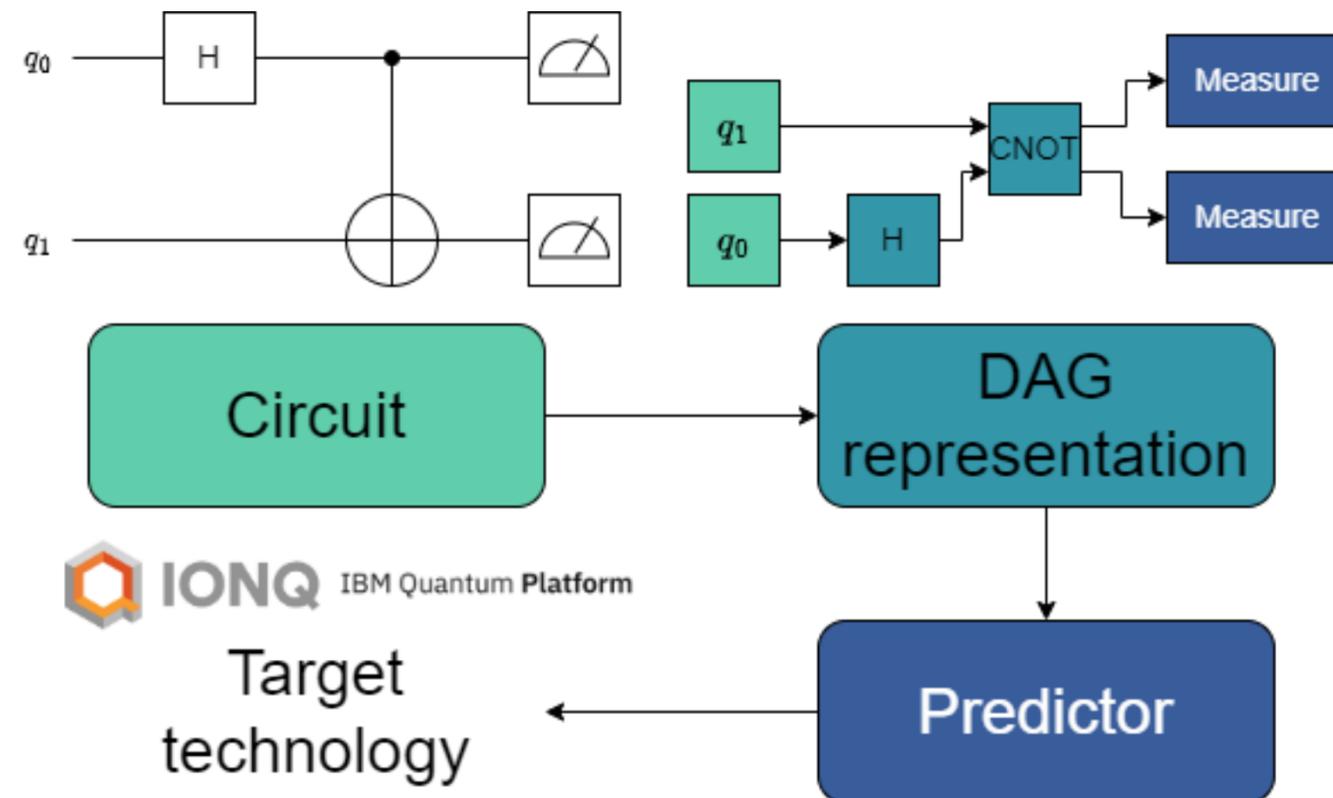


Machine Learning for Quantum Computing

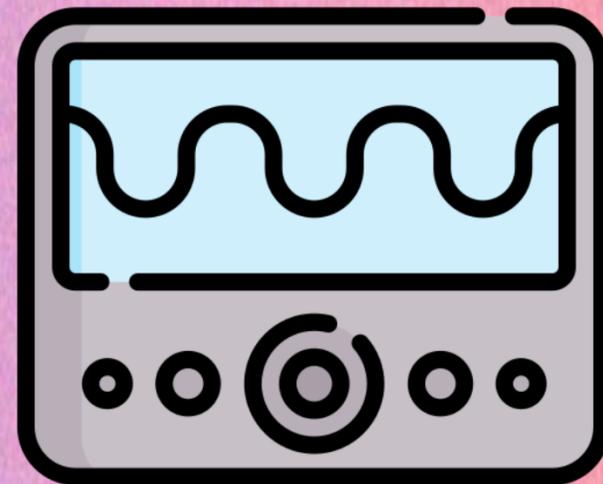


Machine Learning for Quantum Computing

Machine learning is increasingly becoming a key support in quantum technologies, supporting tasks that range from improving quantum hardware performance to optimizing quantum algorithms. As quantum systems scale, the role played by machine learning in quantum computing is expected to grow even stronger, providing essential tools for automation, robustness, and performance optimization.

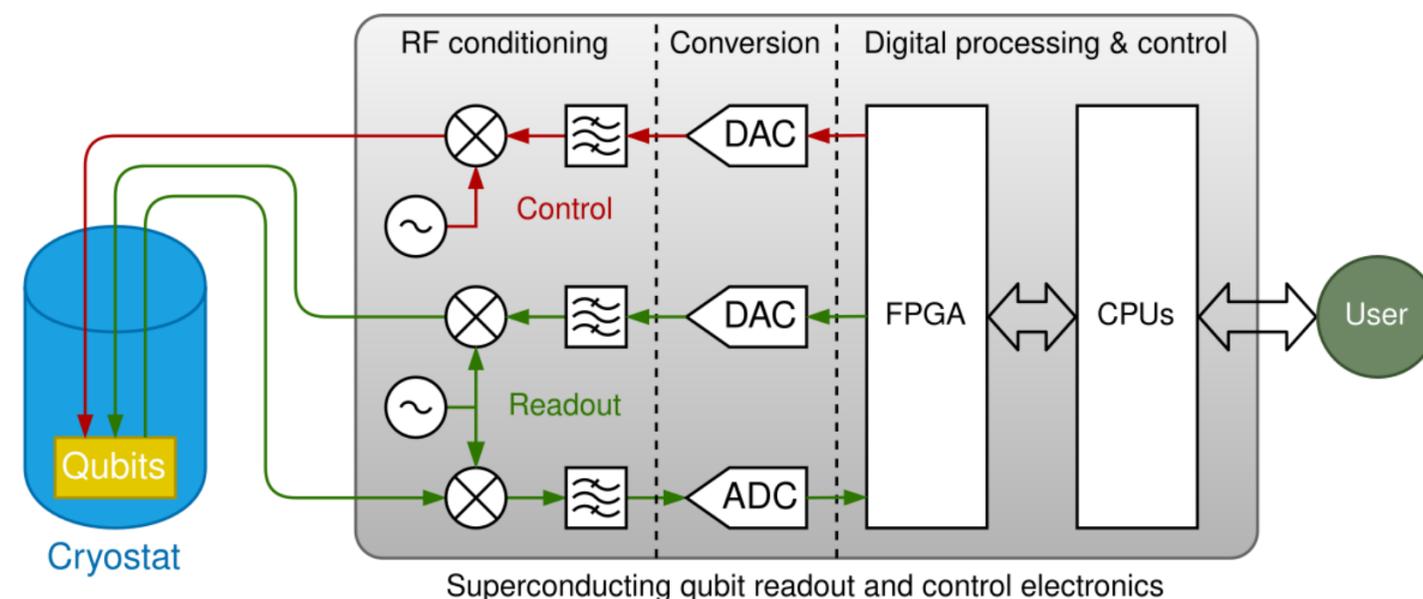


Qubit Control



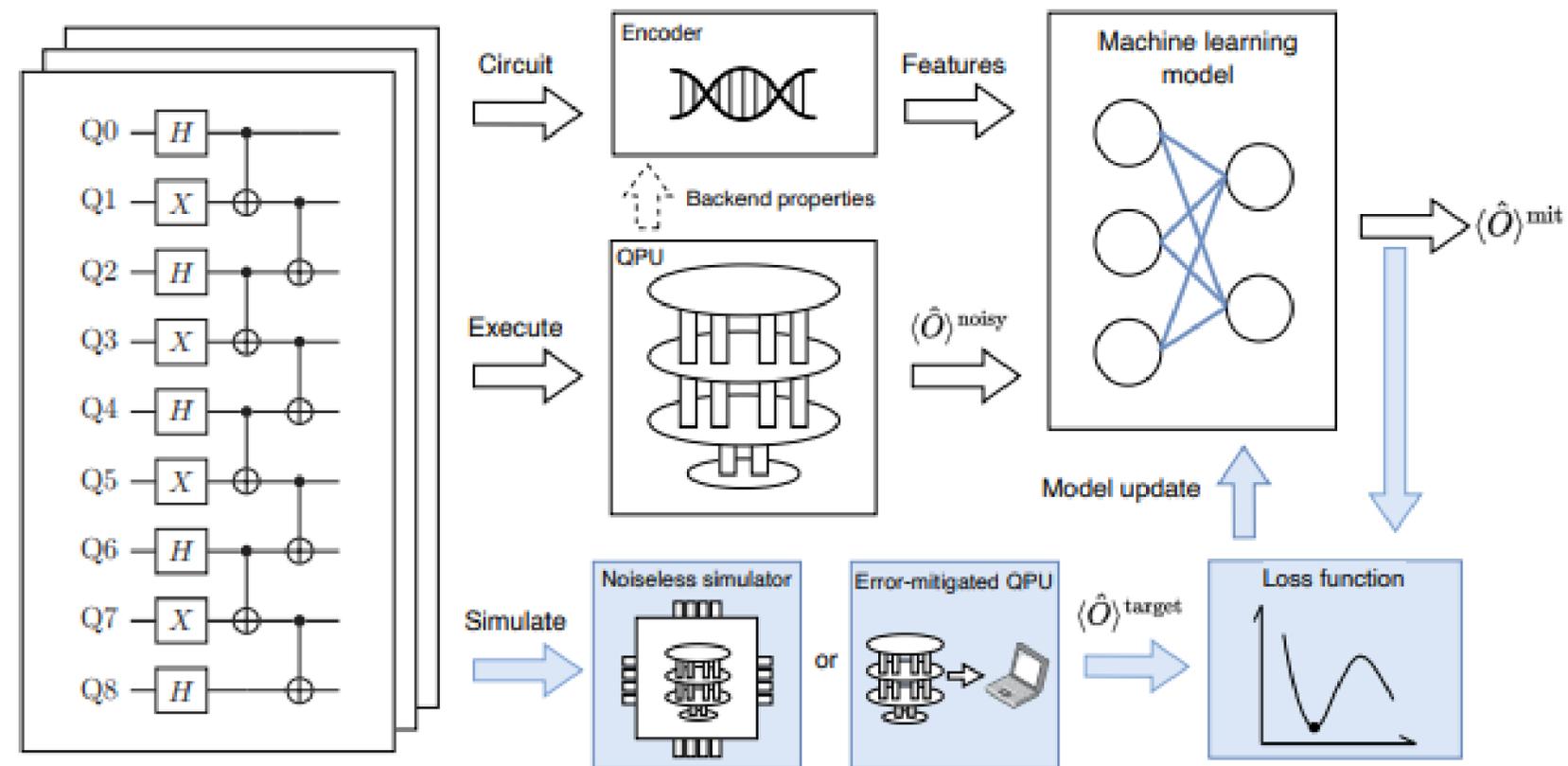
Qubit Control & Readout

Implementation of FPGA architecture for generation of RF signals necessary for controlling superconducting qubits. They are circuits made of superconducting materials, which lose their electrical resistance abruptly below a critical temperature. At the same time, quantum physical effects occur, which give the quantum bit the necessary properties. While the information is stored in the quantum state of the qubits, operations take place in the form of external electromagnetic signals able to change the state of the quantum bits. Typical properties of the pulses are frequencies of several gigahertz and pulse durations in the nanosecond range. A reliable readout of the qubit states is also performed by microwave pulses and their subsequent evaluation.



On-board Error Mitigation

To address the inherent noise of qubits, which significantly affect computational fidelity, this thesis aims to explore machine-learning-based enhancement of the readout stage in quantum control systems to improve measurement accuracy, stability, and noise robustness.



Liao, H., Wang, D. S., Sitdikov, I., Salcedo, C., Seif, A., & Mineev, Z. K. (2024). [Machine learning for practical quantum error mitigation](#). Nature Machine Intelligence, 6(12), 1478-1486.

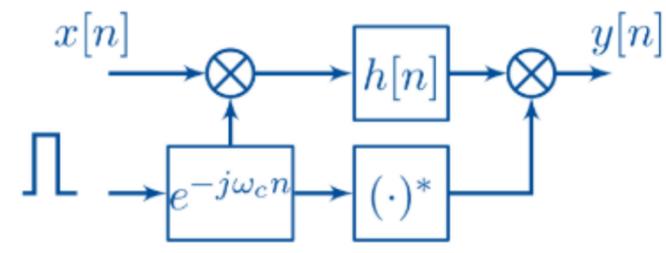
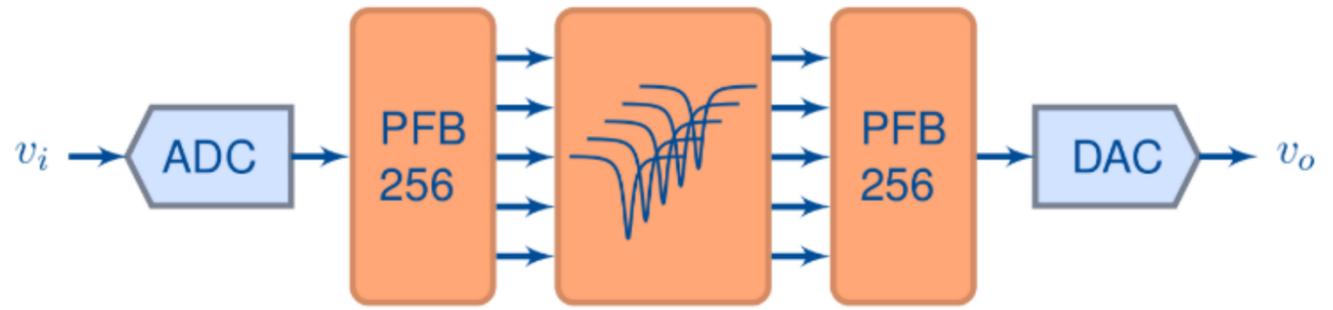
Phuttitarn, L., Becker, B., Chinnarasu, R., Graham, T., & Saffman, M. (2024). [Enhanced measurement of neutral-atom qubits with machine learning](#). Physical Review Applied, 22(2), 024011.

*In collaboration with the National Institute of Nuclear Physics (INFN)

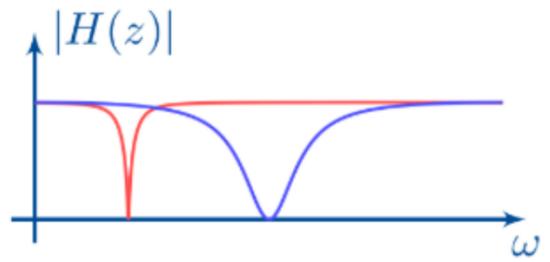
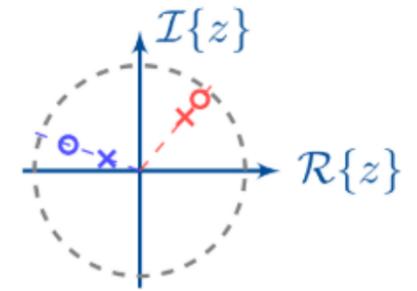
*A thesis on this topic is already active

FPGA-Based Noisy Qubits Emulator

Resonator and Qubit Emulator

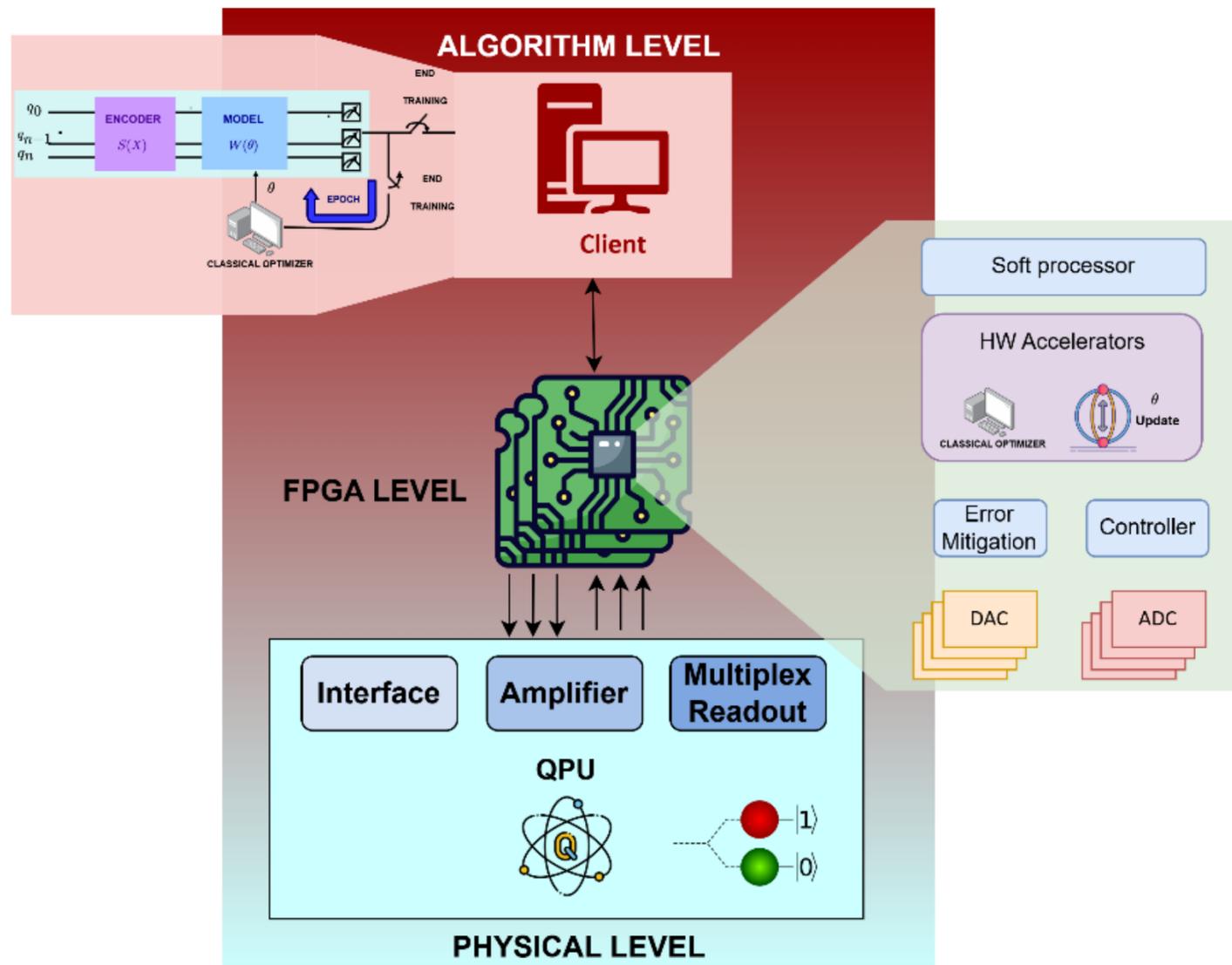


Resonator frequency and Q factor can be adjusted.



Development of physical-level qubit emulator that reproduces the expected measurement outcomes resulting from applied control pulses, providing a response consistent with that of real qubit hardware.

Hardware accelerator for hybrid quantum-classical computing



Development of hardware accelerators for enabling the complete on-board execution of hybrid quantum-classical algorithms for the classical computation components.

In current hybrid algorithms, such as Variational Quantum Algorithms (VQAs), a quantum circuit is iteratively evaluated and updated using classical routines.

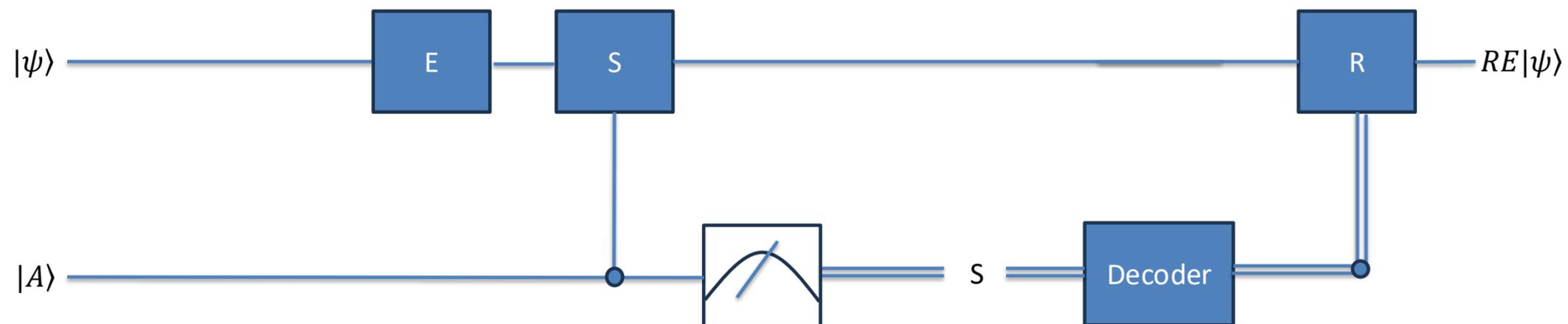
The classical part is performed off-chip, introducing latency and limiting scalability. This thesis wants to address this bottleneck by moving the entire hybrid loop onto the RF-SoC platform, enabling tight coupling between quantum control and classical post-processing.

Error Correction



Error Correction

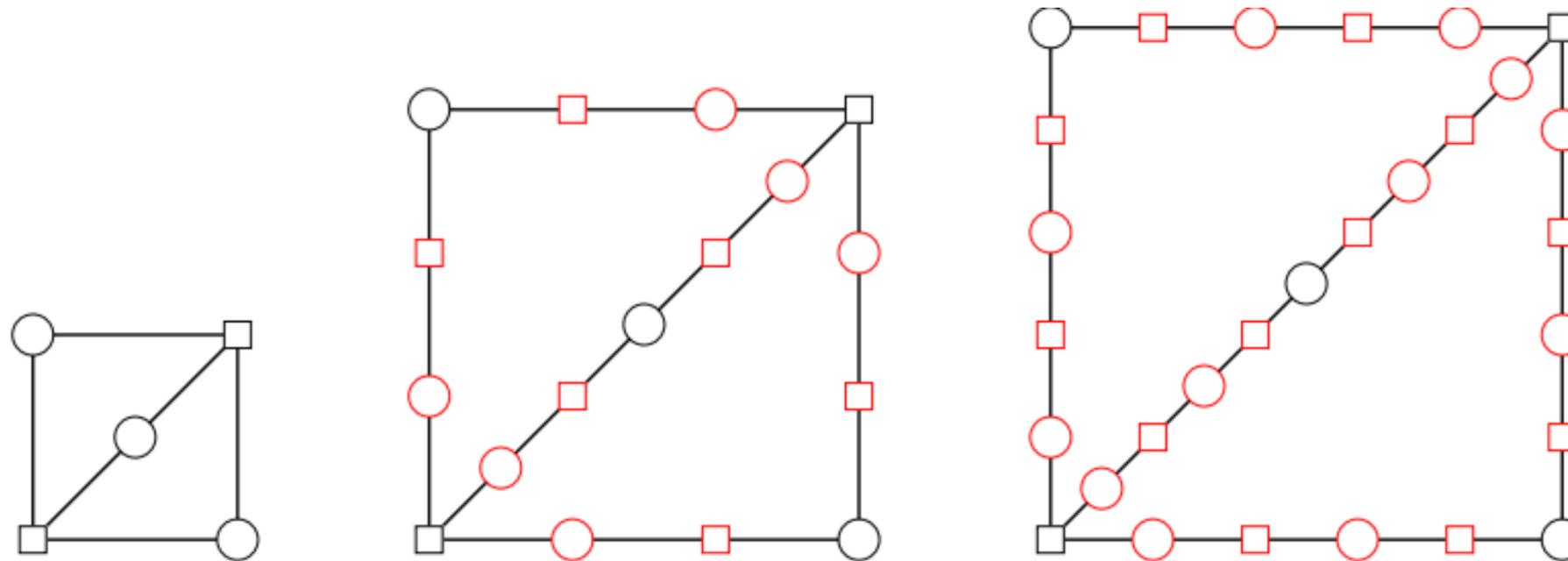
Quantum error correction works by encoding the state of one qubit into several entangled physical qubits, forming a logical qubit. By checking the correlations between these qubits, errors can be detected and corrected without destroying the stored quantum information.



The QEC Cycle: **The Decoder need to be fast!**

Low-Density Parity Check Decoder

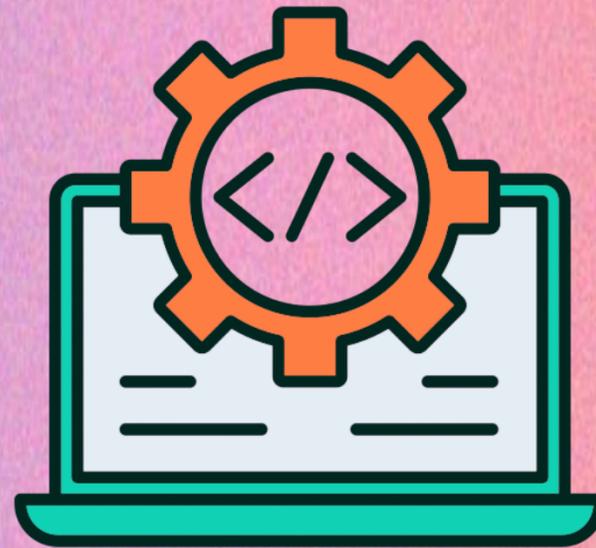
Implement an LDPC (Low-Density Parity-Check) decoder on FPGA, starting from the existing C++ reference implementation of the algorithm provided.



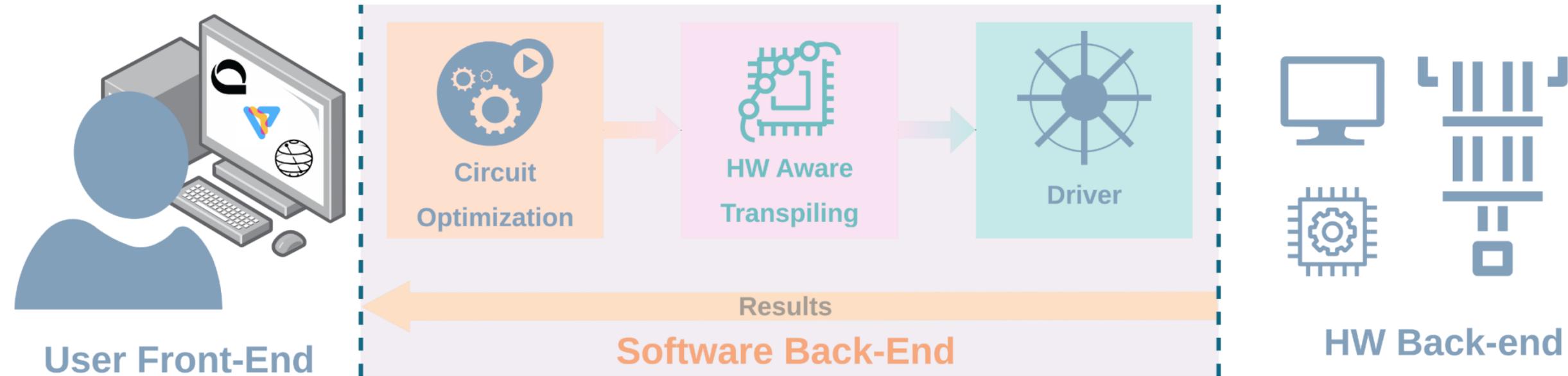
Roffe, Joschka, et al. "[Decoding across the quantum low-density parity-check code landscape](#)." Physical Review Research 2.4 (2020): 043423.

Roffe, Joschka. "[Quantum error correction: an introductory guide](#)." Contemporary Physics 60.3 (2019): 226-245.

Quantum Circuit Compilation



Quantum Circuit Execution Workflow

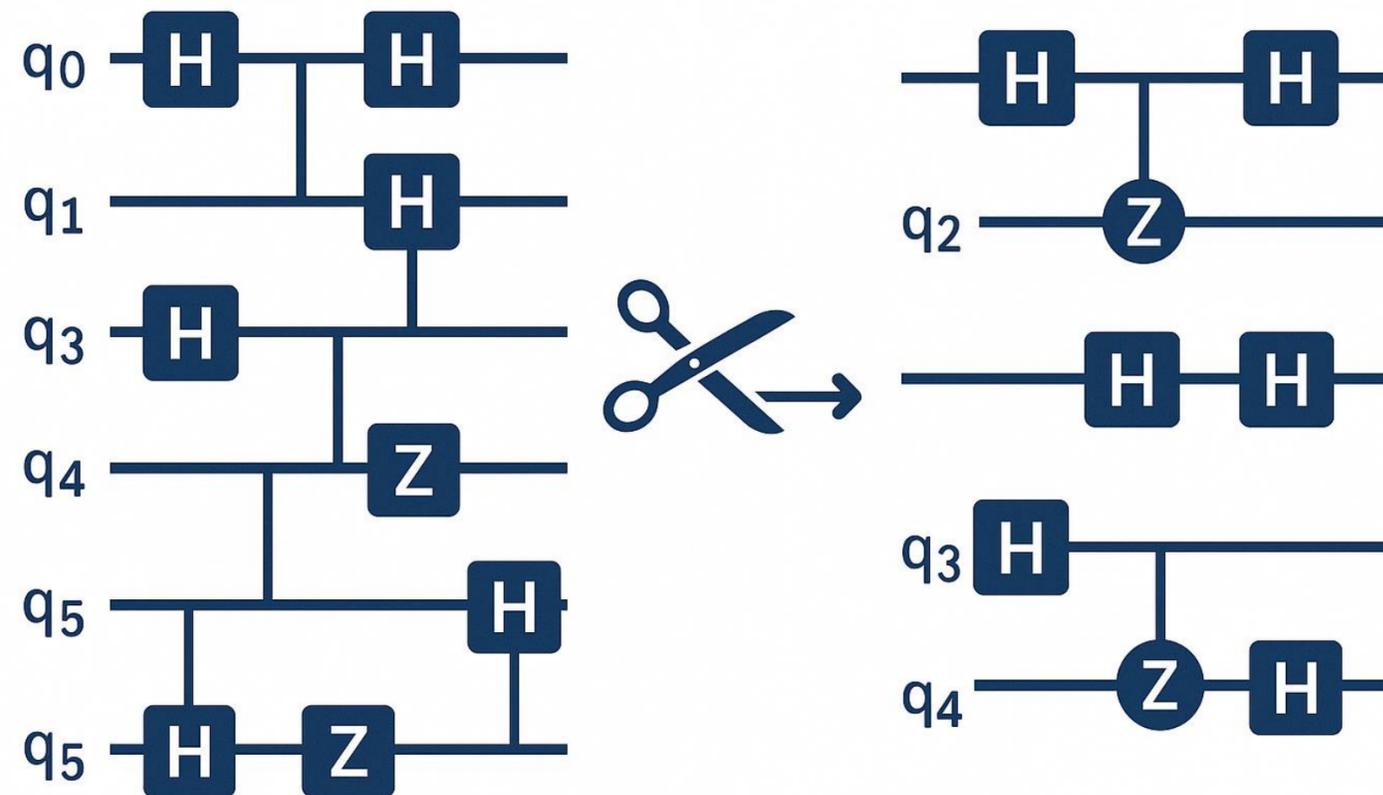


1. Technology constrained circuit optimization
2. Hardware aware circuit mapping
3. Circuit execution
 - QPU
 - CPU/GPU/FPGA

Quantum Circuit Knitting

Starting from SP.3 or from scratch, design an automated lightweight framework that:

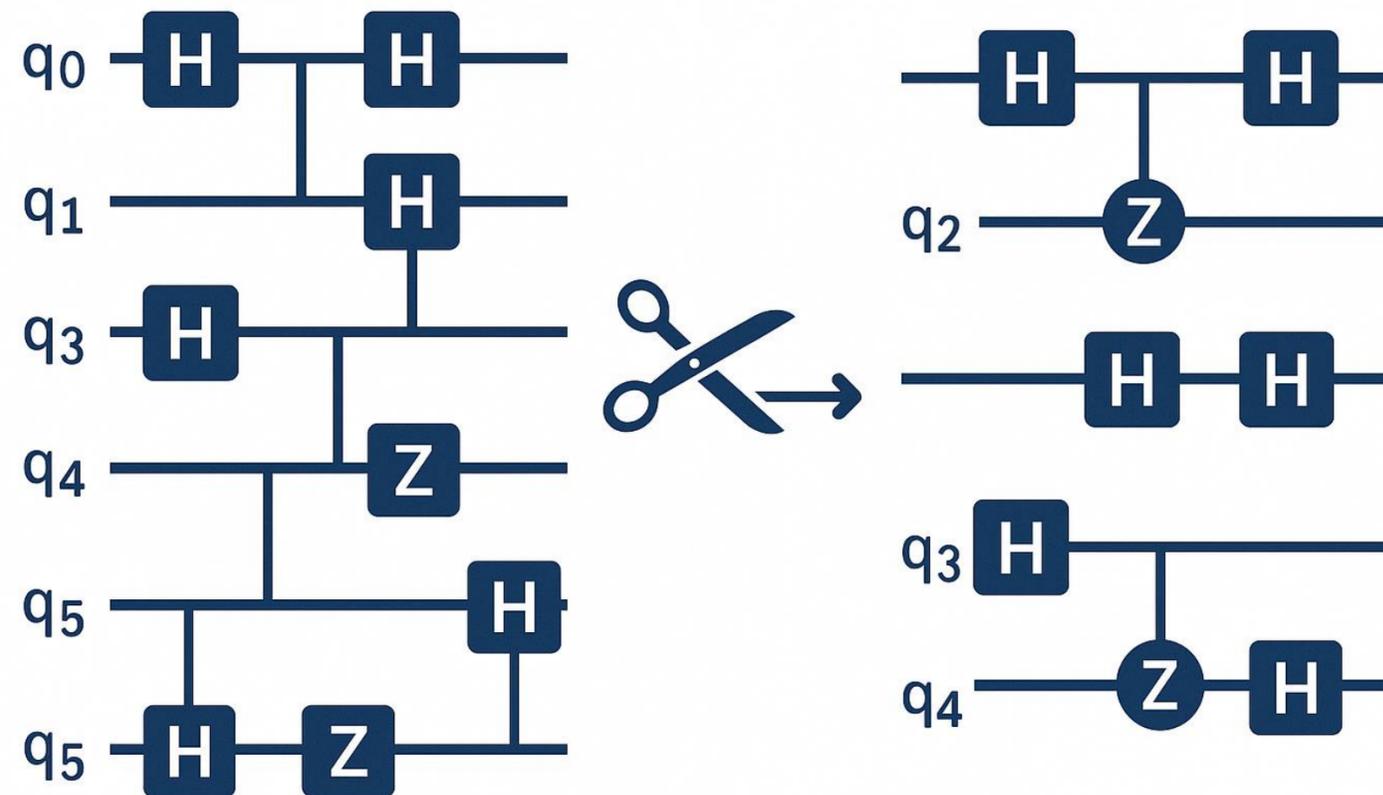
- Identifies the optimal cut of a quantum circuit for a given qubit budget;
- Handle the execution of the resulting subcircuits;
- automatically reconstructs the result from the different runs.



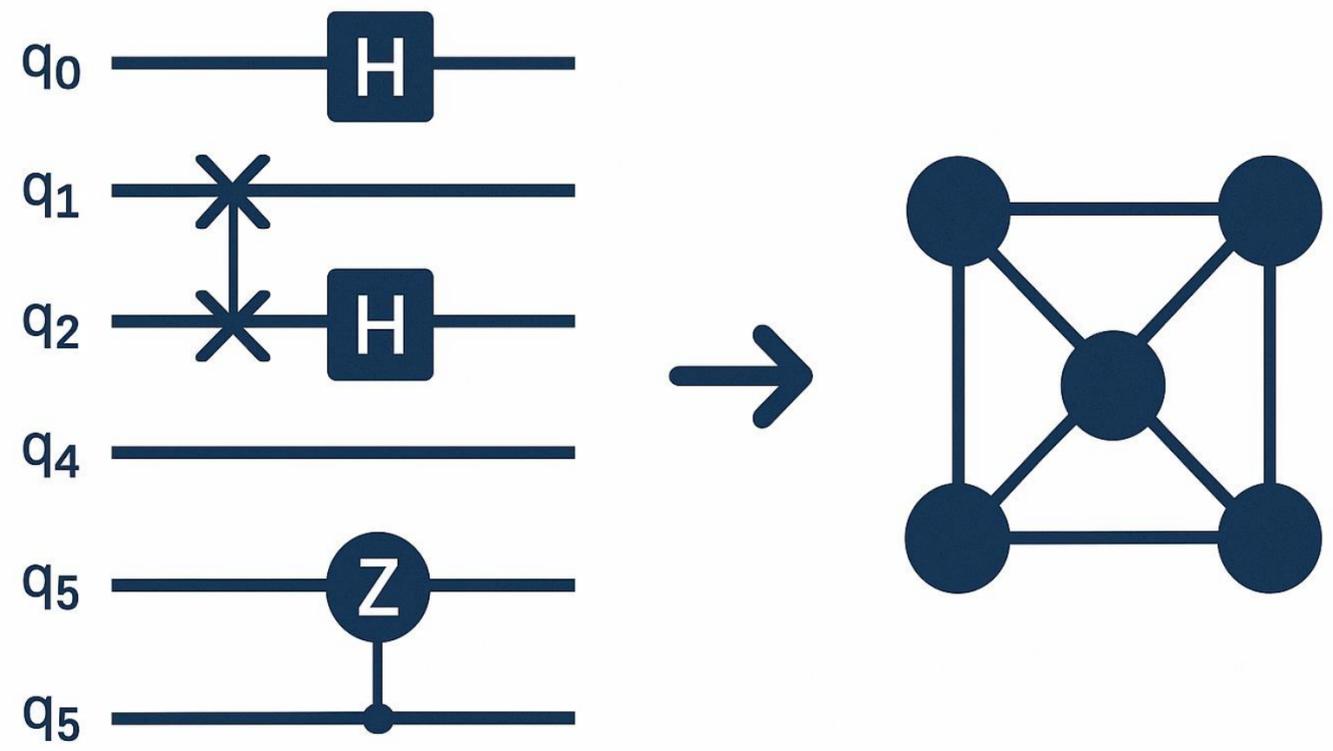
Quantum Circuit Knitting

Starting from SP.3 or from scratch, design an automated lightweight framework that:

- Identifies the optimal cut of a quantum circuit for a given qubit budget;
- Handle the execution of the resulting subcircuits;
- automatically reconstructs the result from the different runs.



Technology Compilation

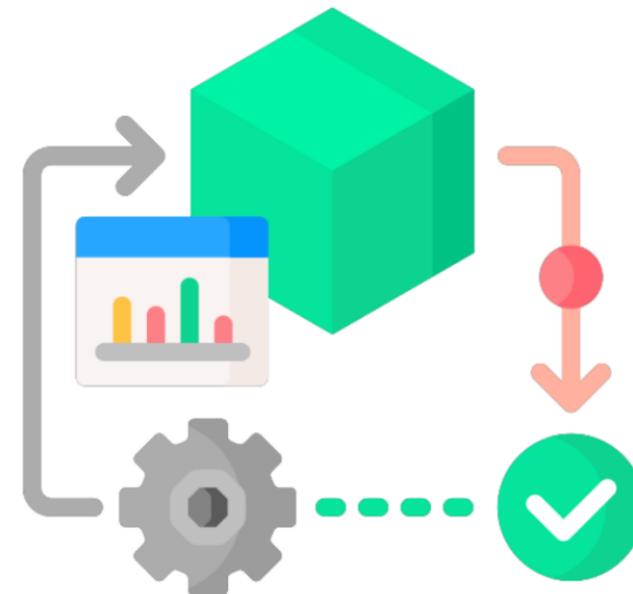


Starting from SP.4 or from scratch, develop a module that performs optimal mapping of a quantum circuit, targeting a given technology, onto a real QPU with a well-defined topology and device characterization.

Avitabile, Manfredi, et al. "[Development of a multi-technology, template-based quantum circuits compilation toolchain.](#)" Quantum Information Processing 21.11 (2022): 379.
 Russo, Andrea, et al. "[Exploring the Advantages of Layout Procedure with Fully-Connected Quantum Computing Technologies.](#)" Advanced Quantum Technologies 7.1 (2024): 2300128.

Hardware-Aware Mapping Optimization on a Superconducting QPU (Lagrange Platform)

- Develop and experimentally validate hardware-aware mapping strategies tailored to the 5-qubit star-topology IQM Spark system.
- **Research Focus**
 - Study the impact of physical constraints (connectivity, T1/T2, gate fidelities, readout quality) on logical-to-physical qubit assignment.
 - Compare ideal simulator-based mappings with hardware-aware mappings executed on Lagrange.
- Quantify trade-offs between:
 - circuit depth
 - exposure to noise



In collaboration with:

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Hardware-Aware Mapping Optimization on a Superconducting QPU (Lagrange Platform)

- **Methodology**

- Extract calibration data from Lagrange (coherence times, gate fidelities, coupling map).
- Implement and benchmark selected
- Evaluate performance under different mapping strategies.
- Propose mapping heuristics guided by real physical metrics.

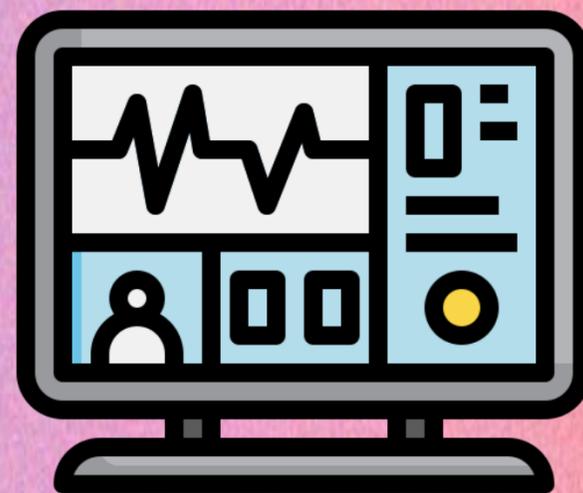
- **Expected Outcomes**

- A validated hardware-aware mapping workflow for small-scale superconducting QPUs.
- Experimental evidence of performance gains over topology-agnostic mapping.
- Guidelines for integrating mapping strategies into compilation toolchains.

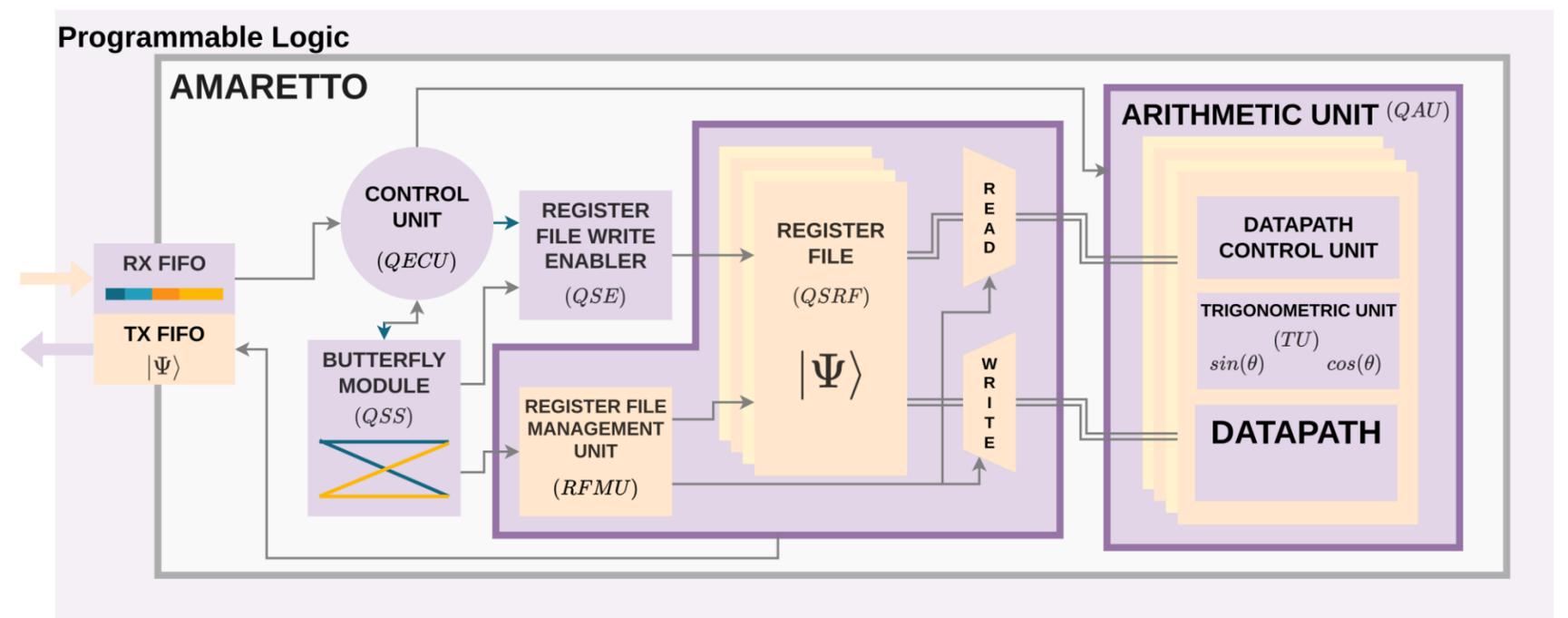
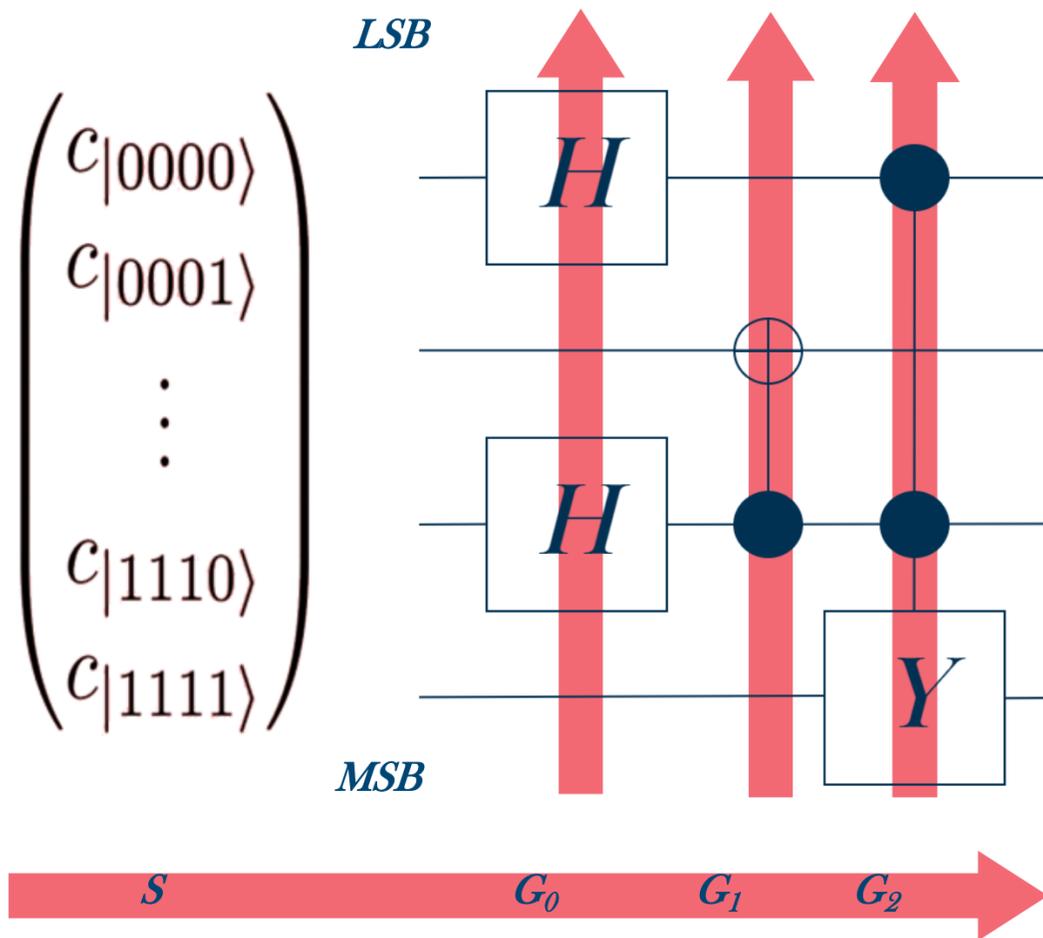
- **Impact:** Bridges quantum algorithm design and physical hardware constraints, reinforcing a system-level engineering approach to quantum computing.



Quantum Circuit Simulation/Emulation



Quantum Circuit Emulation

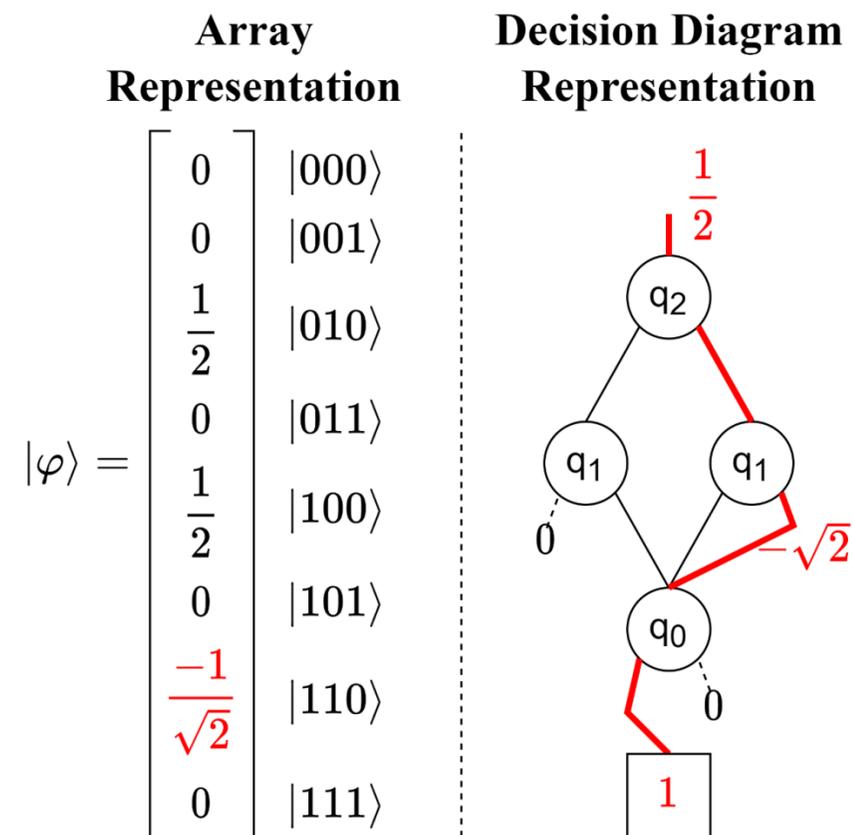


1. Evaluation of quantum circuit evolution in:

- CPU/GPU/FPGA

Quantum Circuit Simulation DD

Starting from SP.2 or from scratch, develop a decision-diagram-based quantum circuit simulator and evaluate optimization and parallelization techniques for execution on CPU, GPU, and NPU platforms.





For any information or curiosity write to:

qnano@polito.it